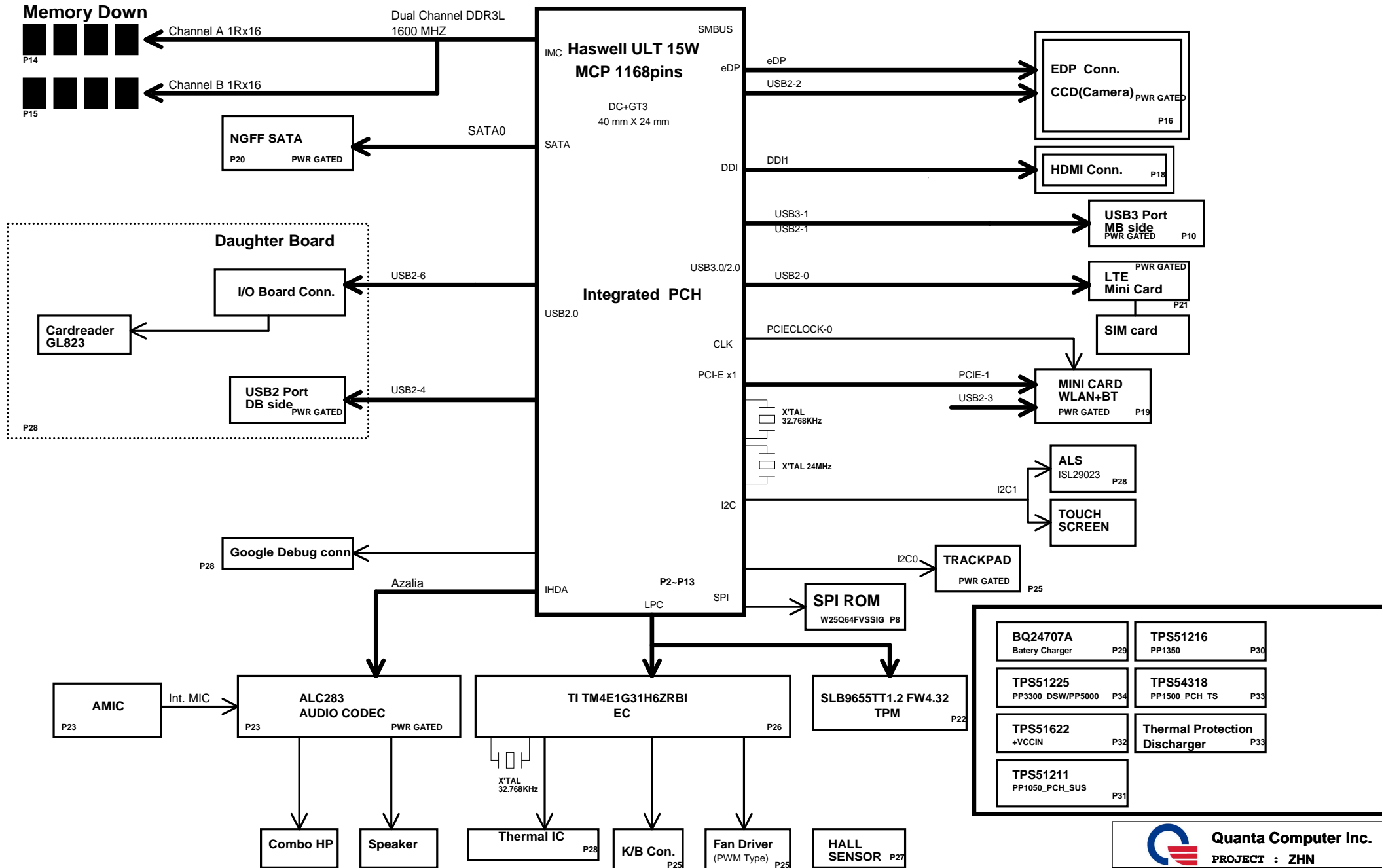


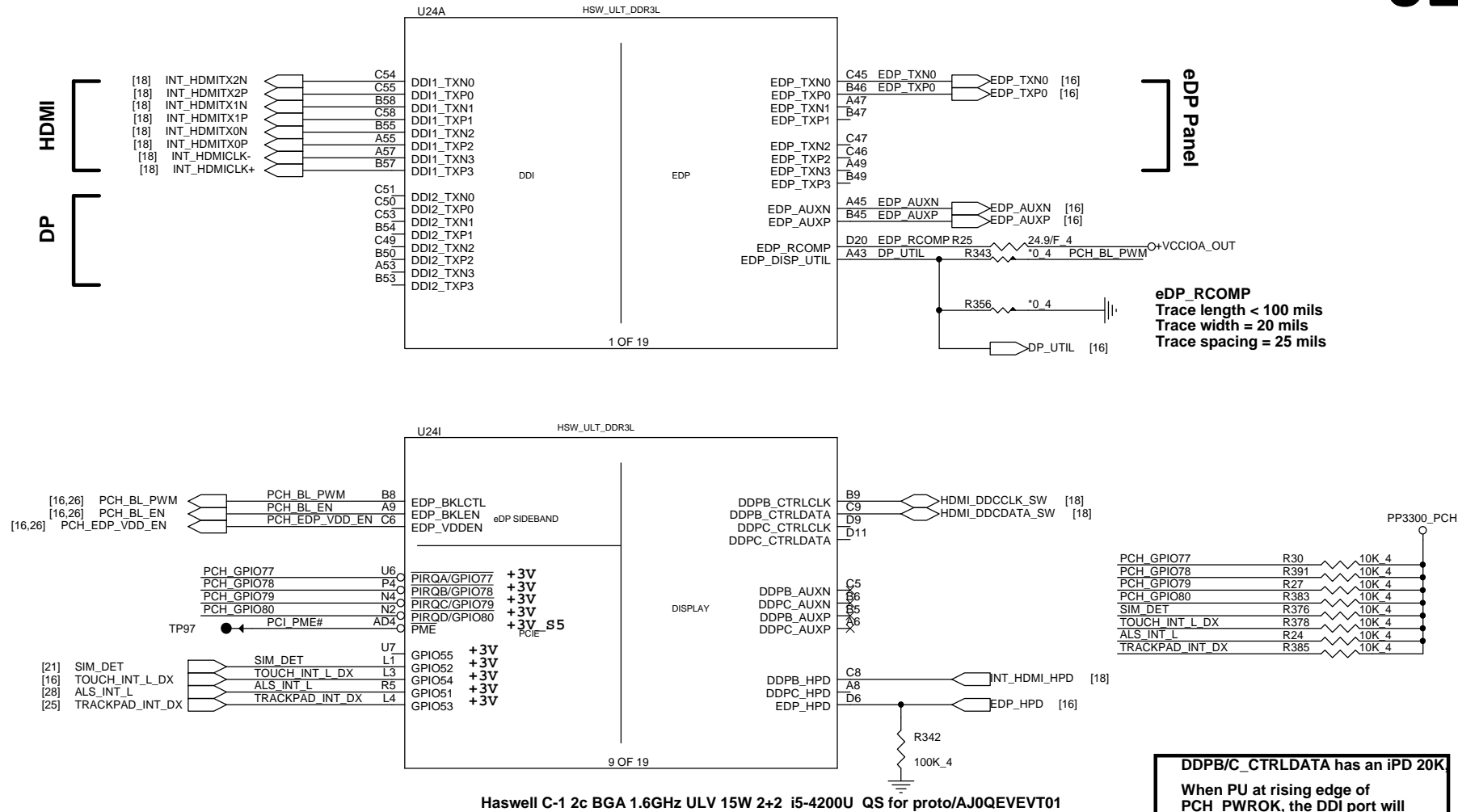
ZHN SHB ULT SYSTEM BLOCK DIAGRAM

01



Haswell ULT (DISPLAY,eDP)

02



DDPB/C_CTRLCLK has an iPD 20K
When PU at rising edge of PCH_PWROK, the DDI port will be detected



Quanta Computer Inc.

PROJECT : ZHN

Size	Document Number	Rev
	Haswell 1/5 (DDI/eDP)	3B
Date:	Monday, August 26, 2013	Sheet 2 of 39

HSW IULT D083

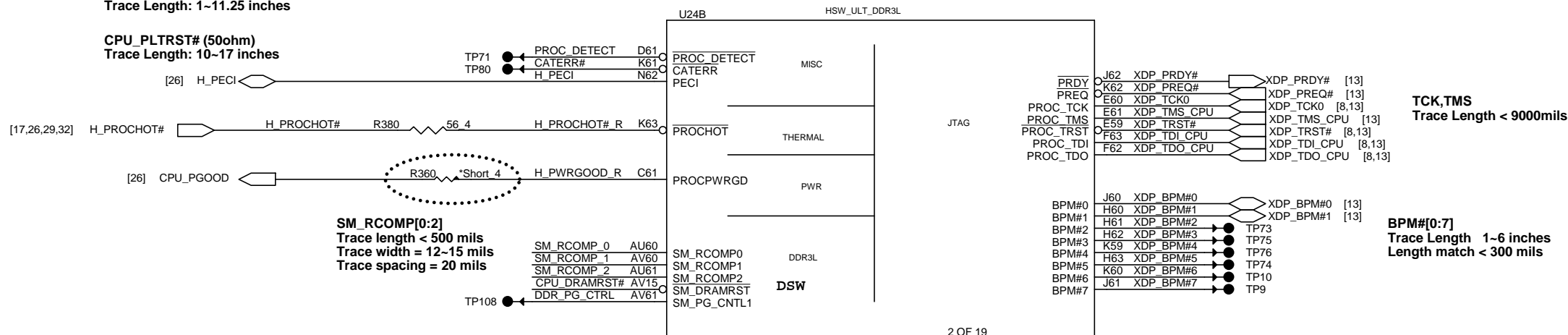


Haswell ULT (SIDE BAND)

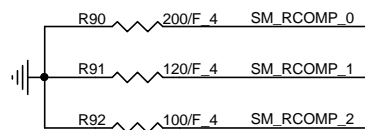
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

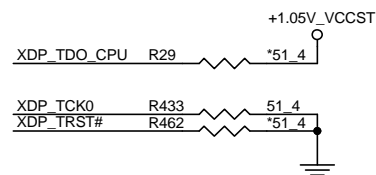
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



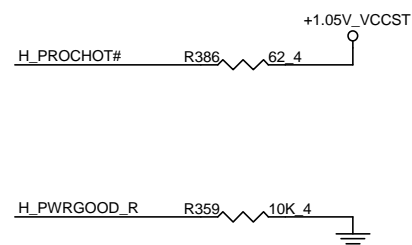
DRAM COMP



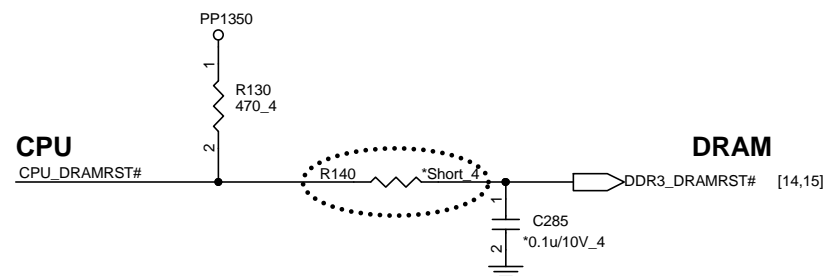
XDP PU/PD



PU/PD of CPU



DRAMRST

**Quanta Computer Inc.**

PROJECT : ZHN

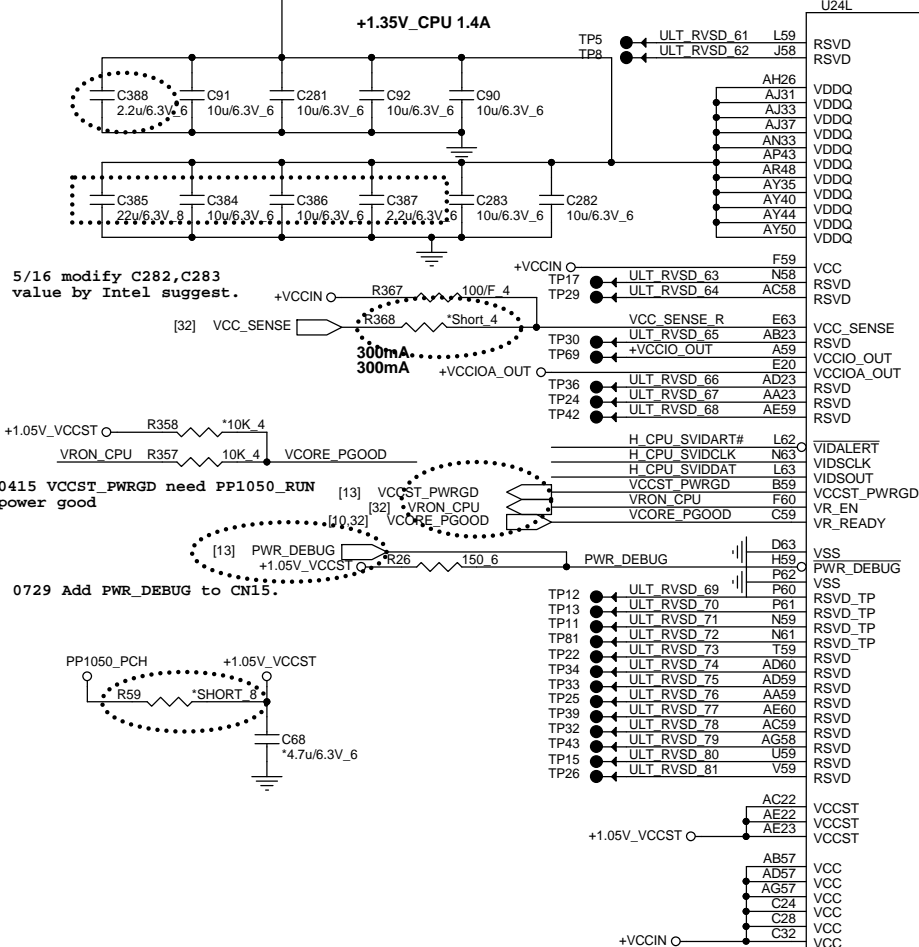
Size	Document Number	Rev
	Haswell 3/5 (SideBand)	3B
Date:	Monday, August 26, 2013	Sheet 4 of 39

Date: Monday, August 26, 2013 Sheet 4 of 39

Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity

6/21 Add C384~C388 by Intel DDR.



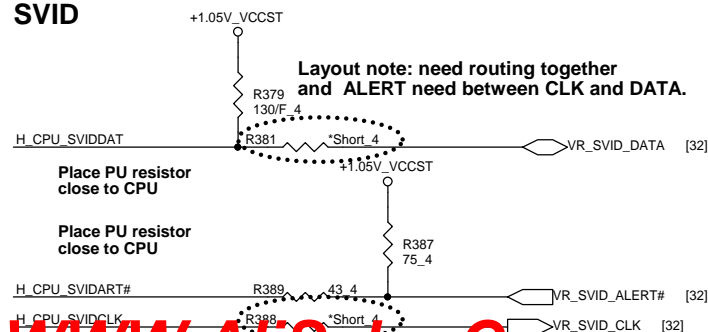
HSW ULT DDR3L

HSW ULT POWER

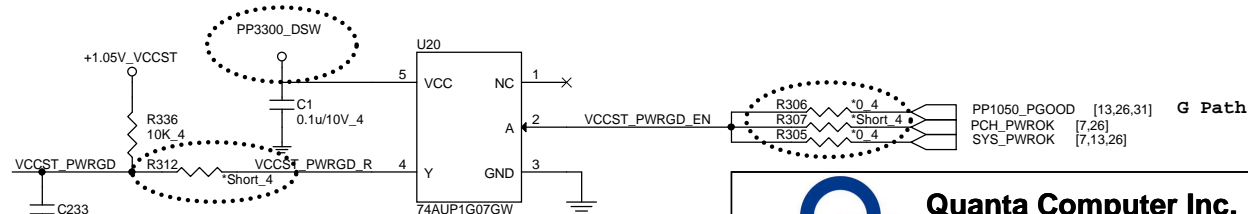
12 OF 19

VCC Output Decoupling Recommendations		
2470FxF4	7343	TOP socket side
22uFxF8	0805	4 on TOP, 4 on BOT near socket edge
22uFxF11	0805	TOP, inside socket cavity
10uFxF11	0805	BOT, inside socket cavity

SVID



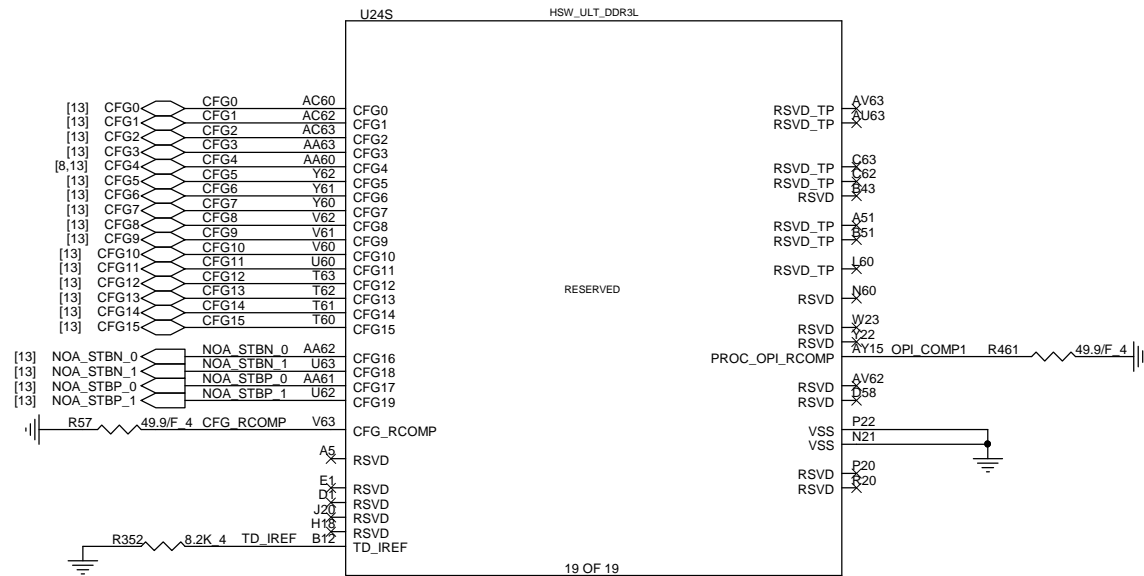
VCCST PWRGD

**Quanta Computer Inc.**

PROJECT : ZHN

Haswell 4/5 (POWER)

Date: Monday, August 26, 2013 Sheet 5 of 39



Processor Strapping

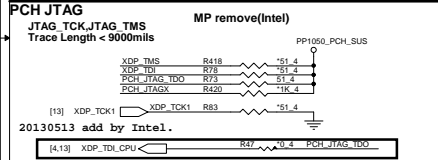
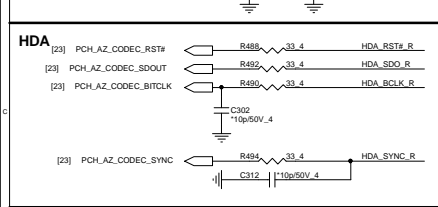
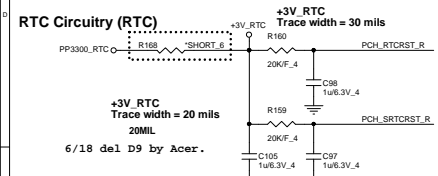
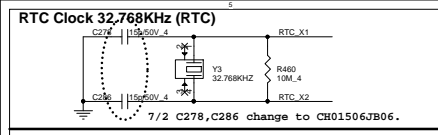
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R417 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R423 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K 4



Quanta Computer Inc.

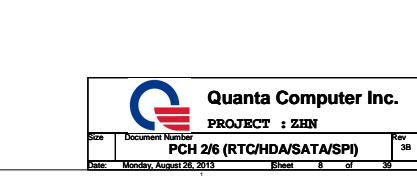
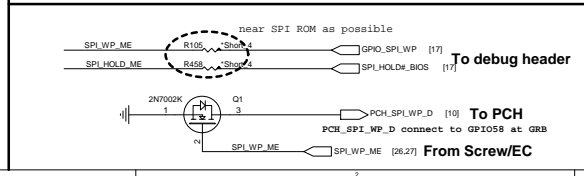
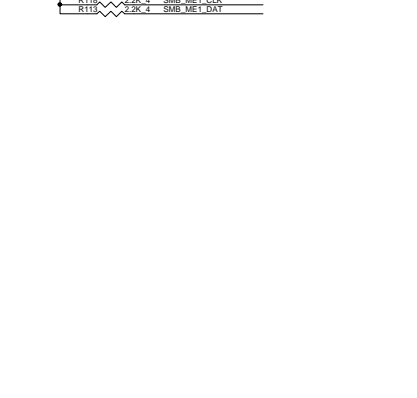
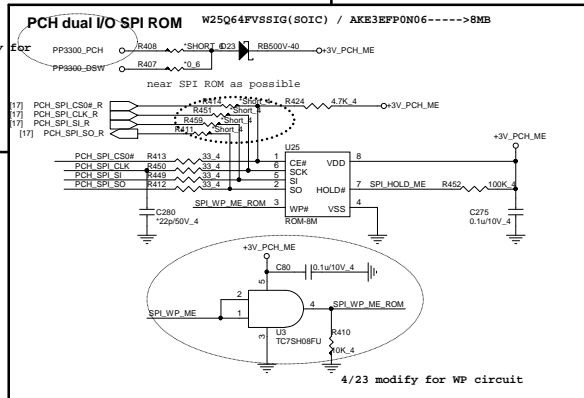
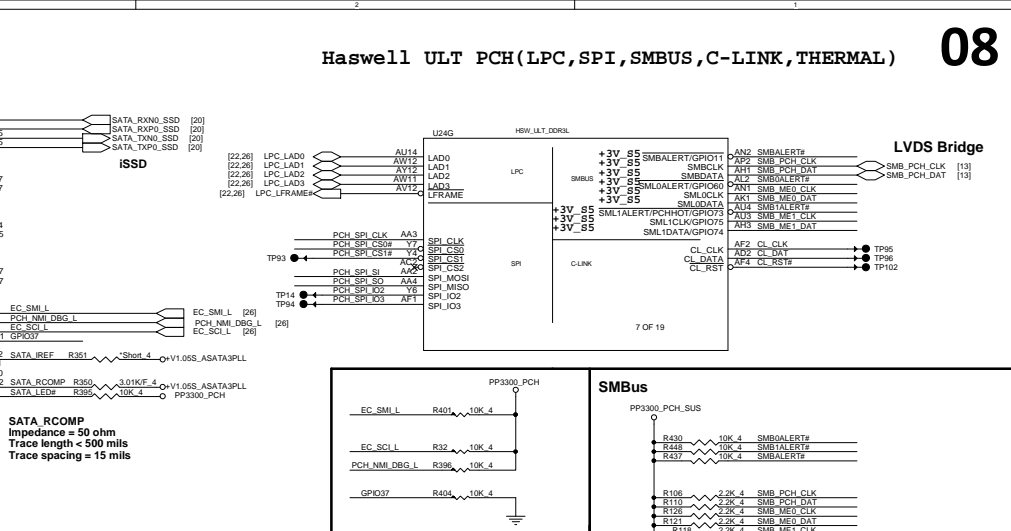
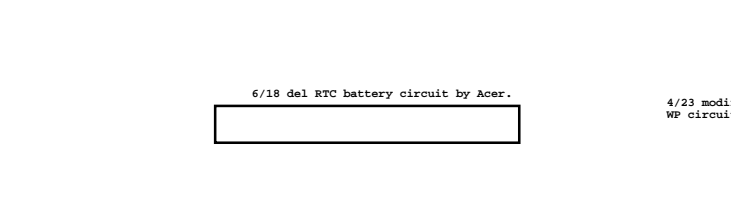
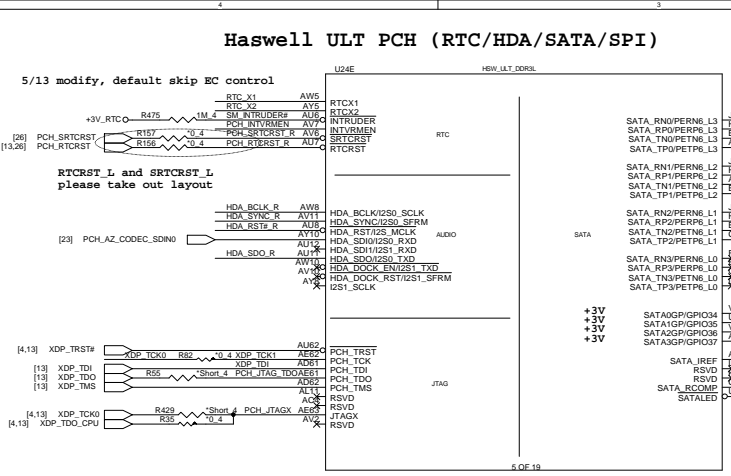
PROJECT : ZHN

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3B
Date:	Monday, August 26, 2013	Sheet 6 of 39



ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode	PP3300_PCH R400 *1K 4 SPKR [10,23]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (IPD 20K) 1 = can't program ME	HDA_SDO_R R493 *0.4 PCH HDA_SDO [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1 = Should be always pull-up	+3V_RTC R484 *330K 4 PCH INTRMEN R486 *330K 4
GPIO66	Top-Block Swap override		0 = Default disable (IPD 20K) 1 = Enable TBS function	PP3300_PCH R330 *1K 4 GPIO66 R340 *1K 4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC	PP3300_PCH R1 *1K 4 GPIO86 R7 *1K 4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality (IPD 20K) 1 = Default enable with confidentiality	PP3300_PCH_SUS R50 *8.2K 4 GPIO15 R58 *1K 4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable	[6,13] CFG4 R64 *1K 4
DSWVREN	Deep Sx well on the VR enable		1 = Should be always pull-up	[7] DSWVREN R476 *330K 4 DSWVREN R472 *330K 4

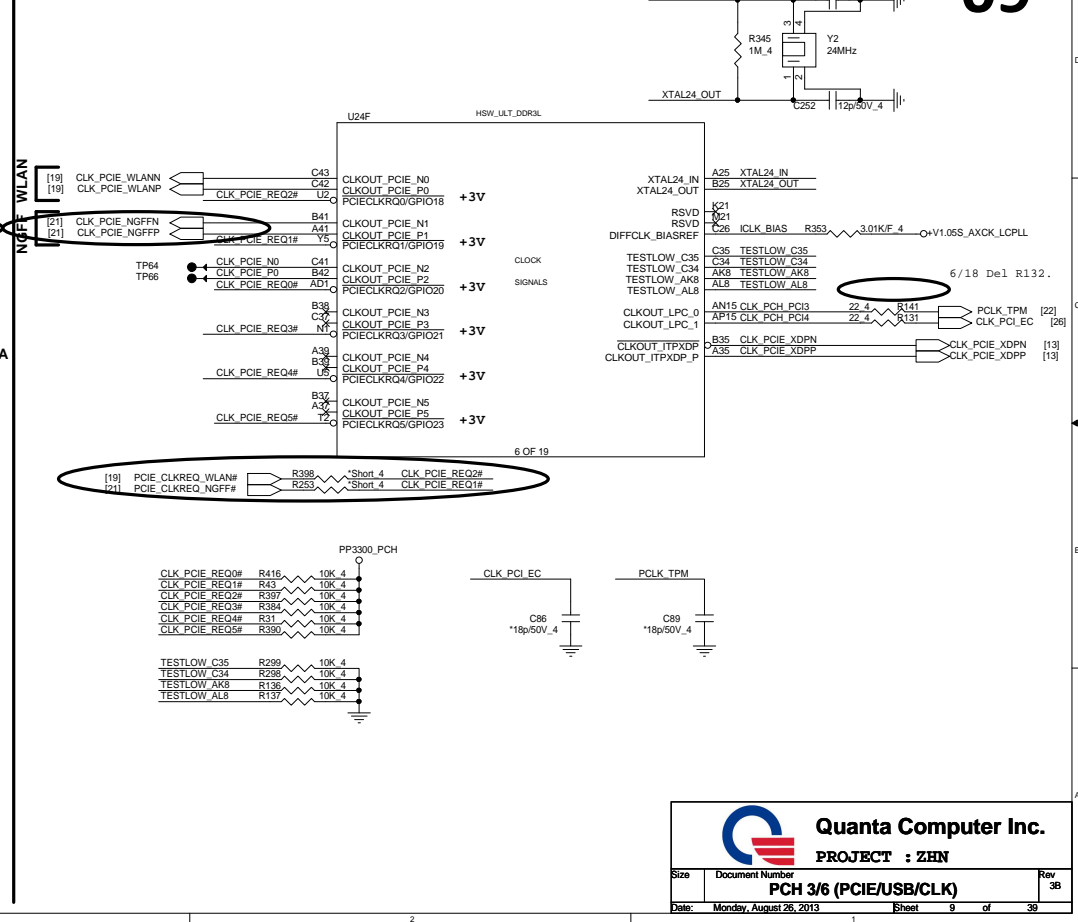
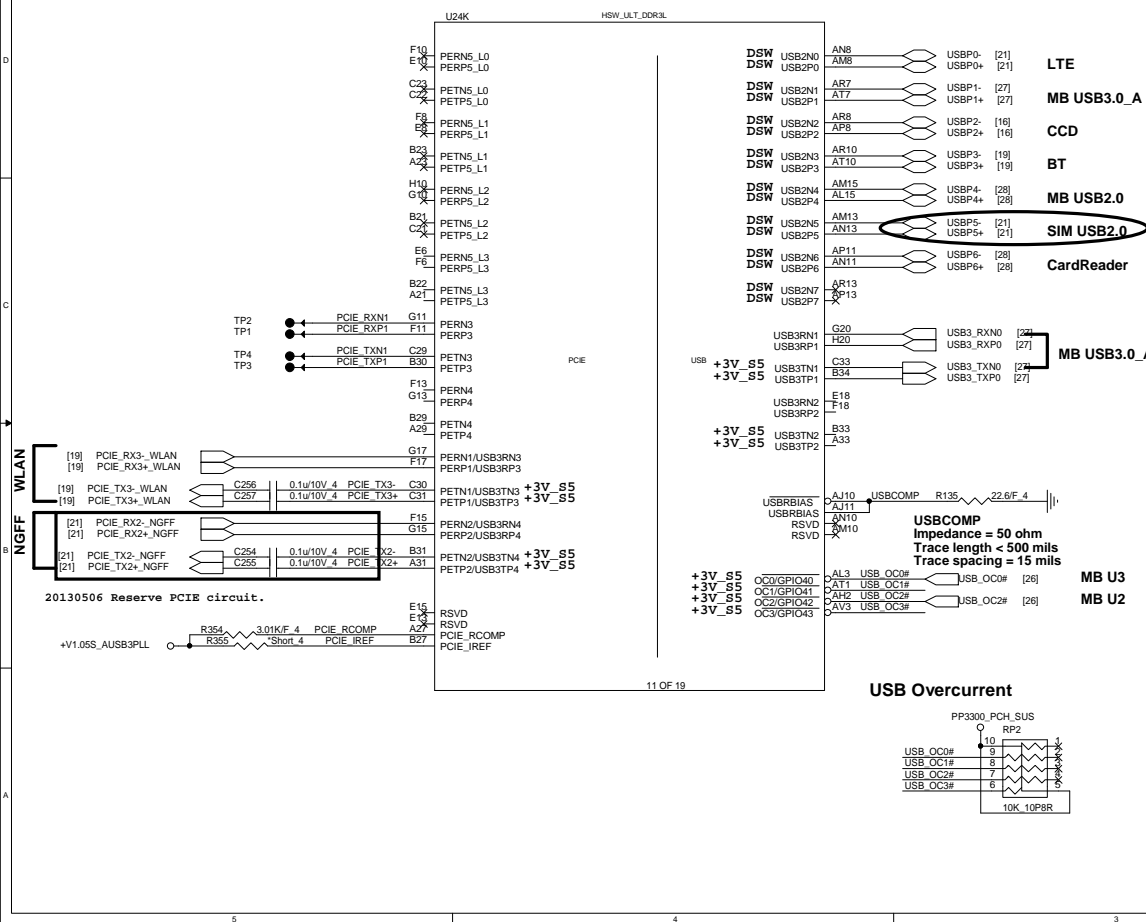


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PROJECT : ZHN
Size Document Number
PCH 2/6 (RTC/HDA/SATA/SPI)
Date: Monday, August 28, 2013 Sheet 8 of 30

Haswell ULT PCH (PCIE,USB3.0,USB2.0)

Haswell ULT PCH (CLOCK)

09

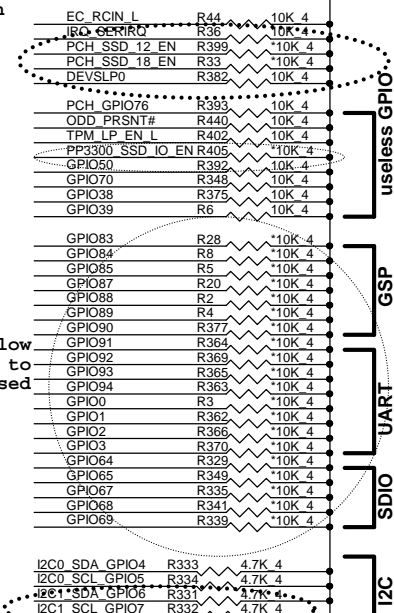


Quanta Computer Inc.
PROJECT : ZHN

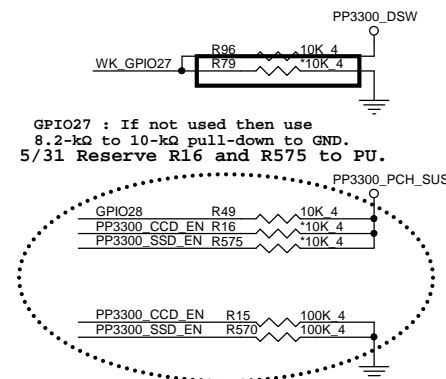
Size	Document Number	Rev
	PCH 3/6 (PCIE/USB/CLK)	3B
Date:	Monday, August 26, 2013	Sheet 9 of 38

10

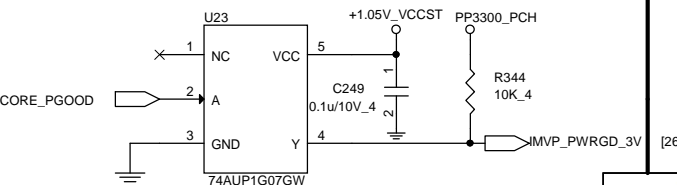
PP3300 PCH



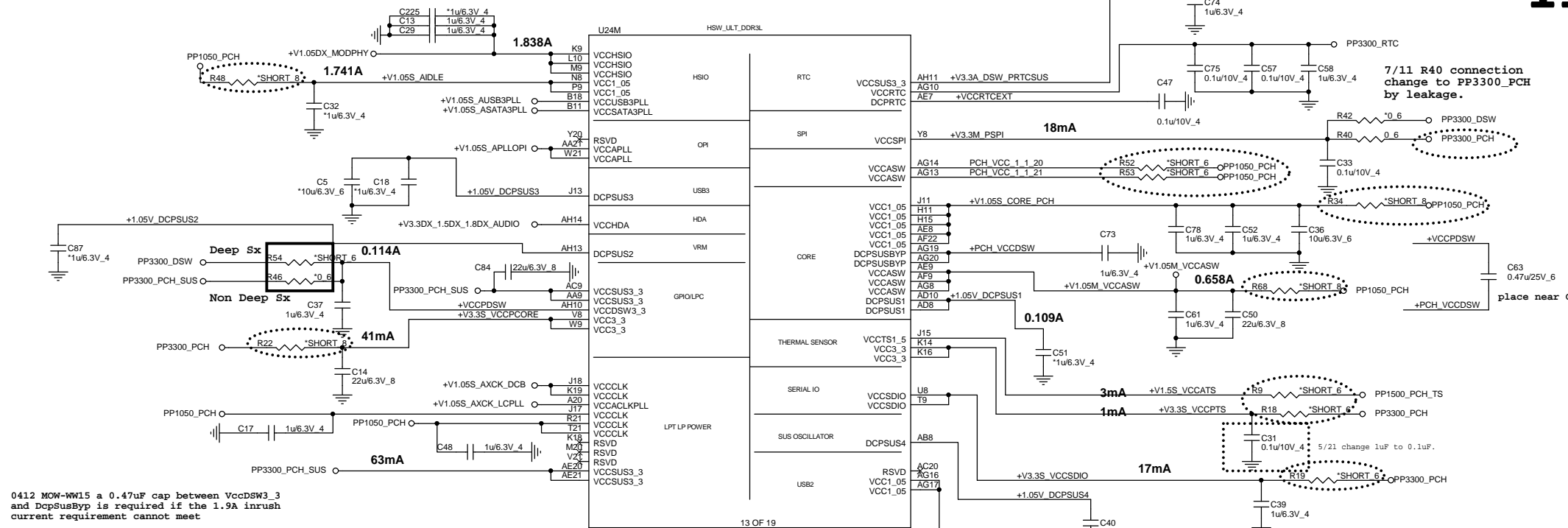
20130613 change R331,R332 to 4.7K.



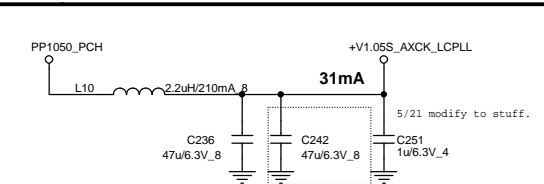
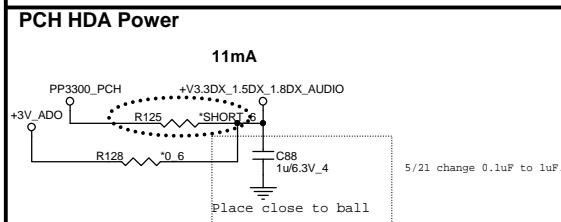
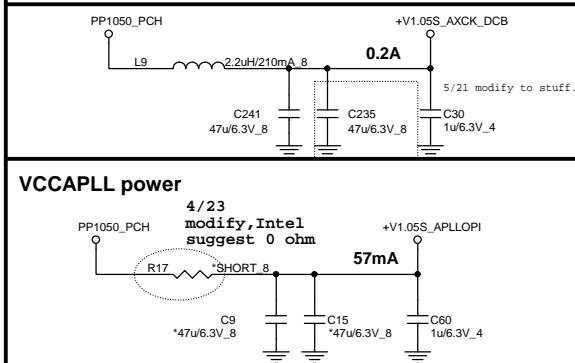
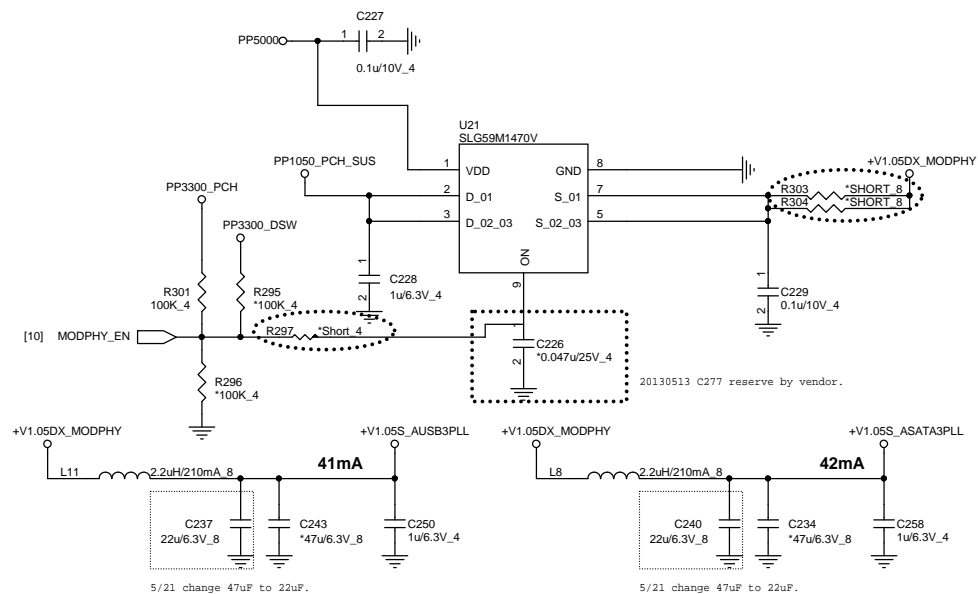
The diagram shows a 2N7002DW MOSFET circuit. The gate is connected to two inputs: PP3300_WLAN_EN (pin 5) and PP3300_LTE_EN (pin 2). The drain is connected to two outputs: WLAN_WAKE_L (pin 4) and LTE_WAKE_L (pin 1). The source is connected to two inputs: WLAN_WAKE_L_Q (pin 3) and LTE_WAKE_L_Q (pin 6). The MOSFET is labeled 2N7002DW.

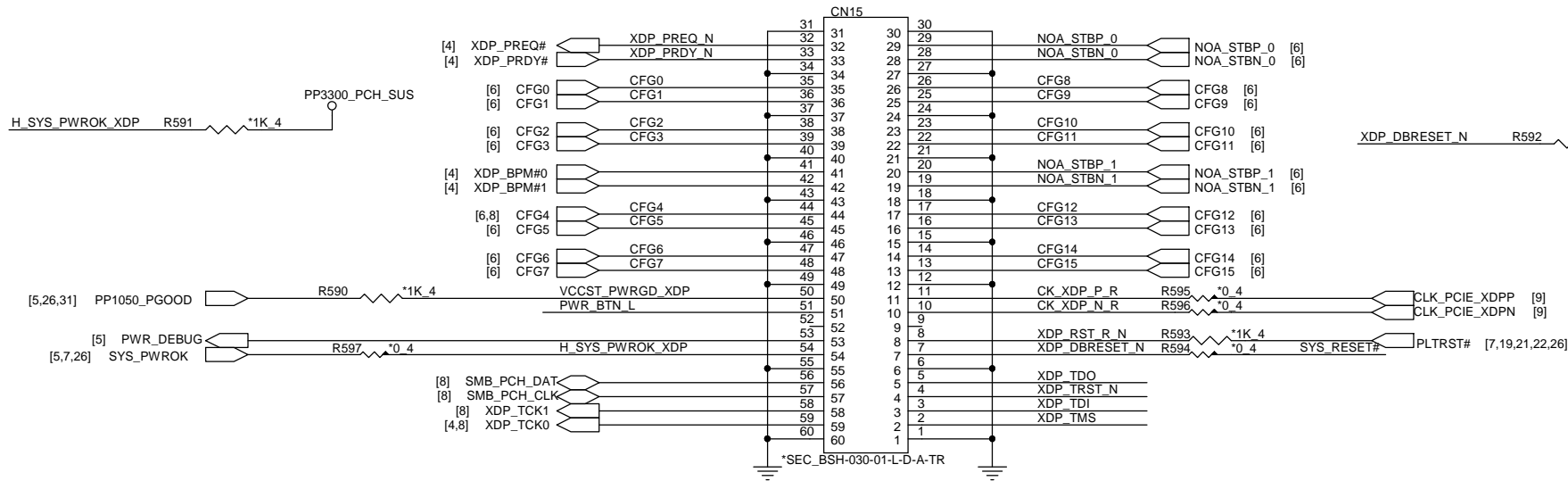


Haswell ULT PCH (Power)

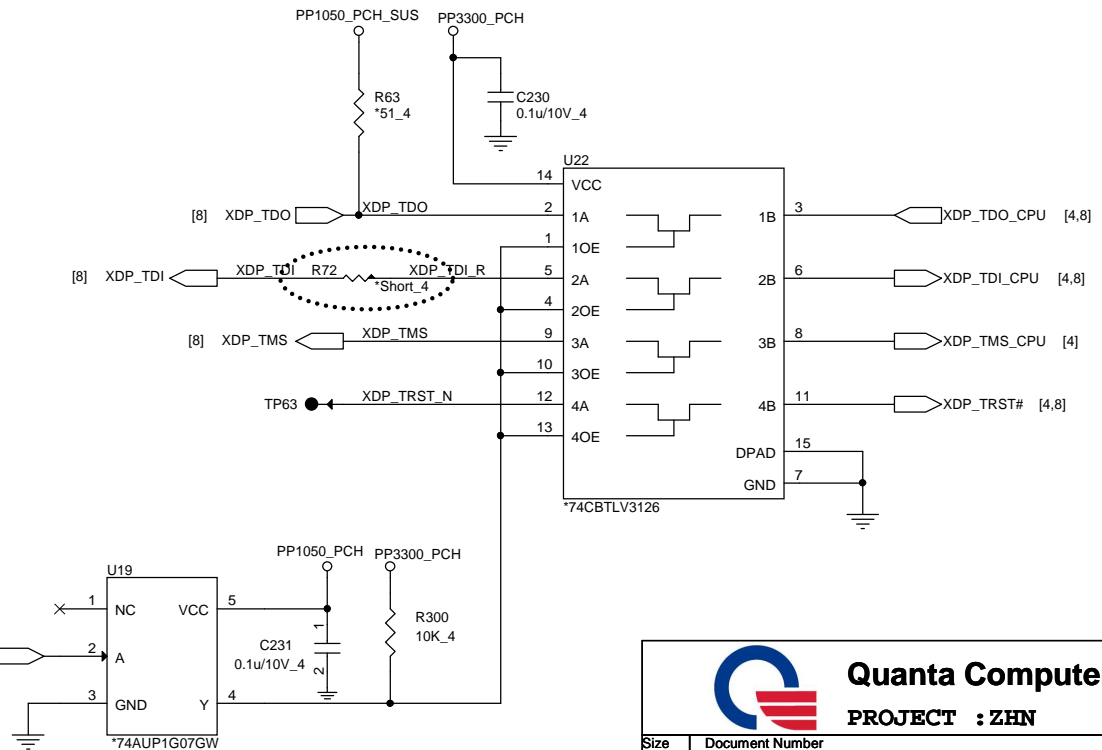
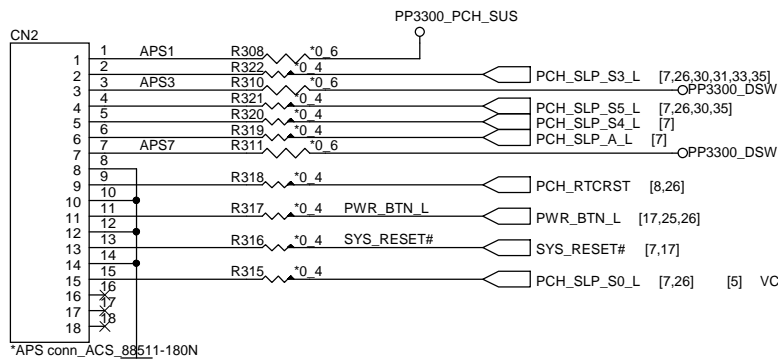


PCH VCCHSIO Power

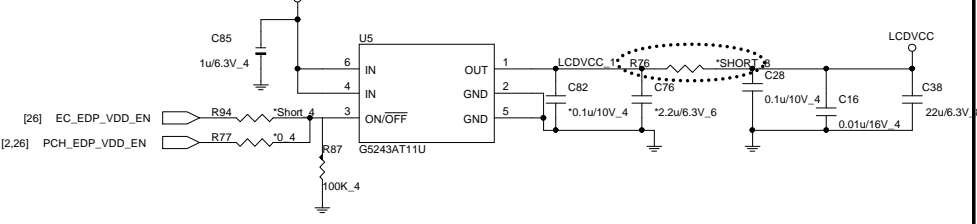




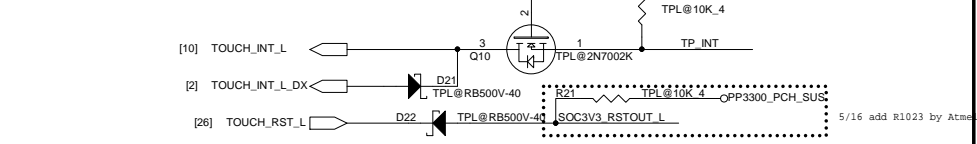
APS



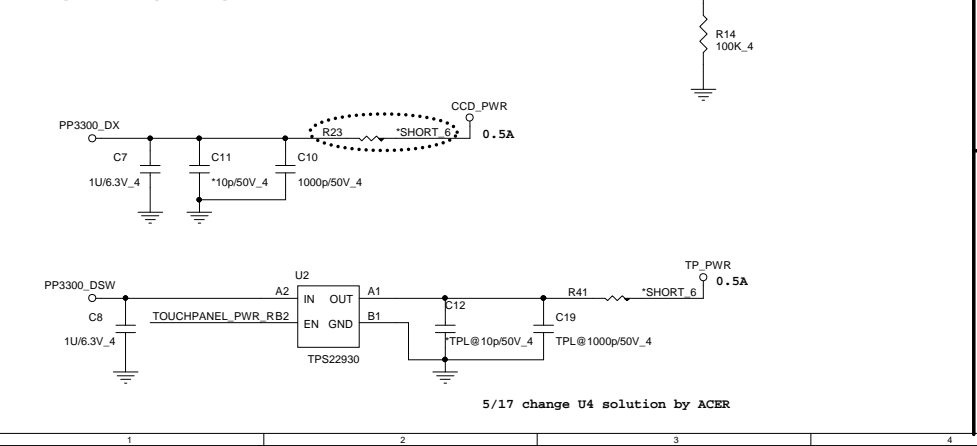
LVDS Power(LDS)



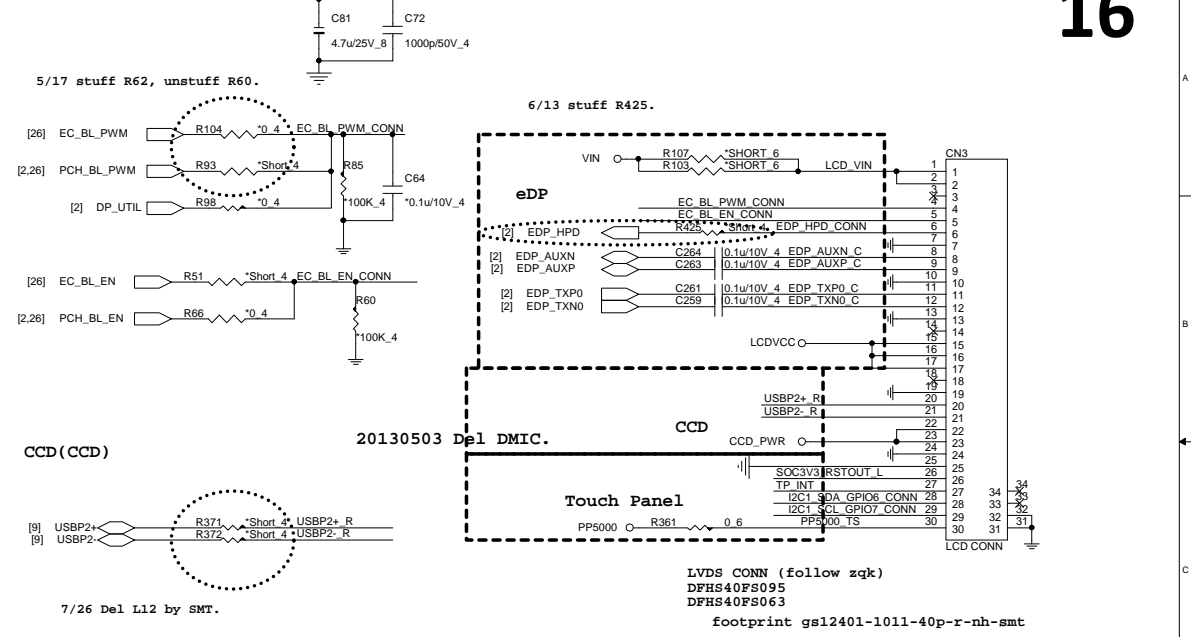
Touch Panel INT/RST(TPS)



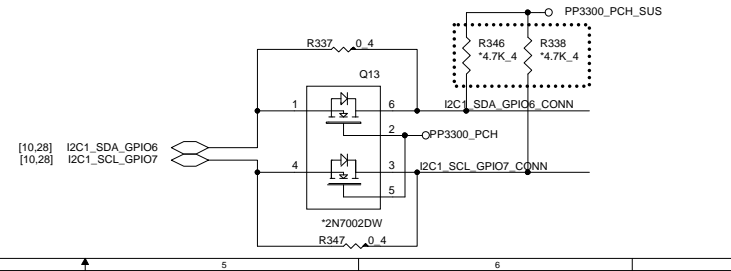
CCD power(CCD)



LVDS(LDS)



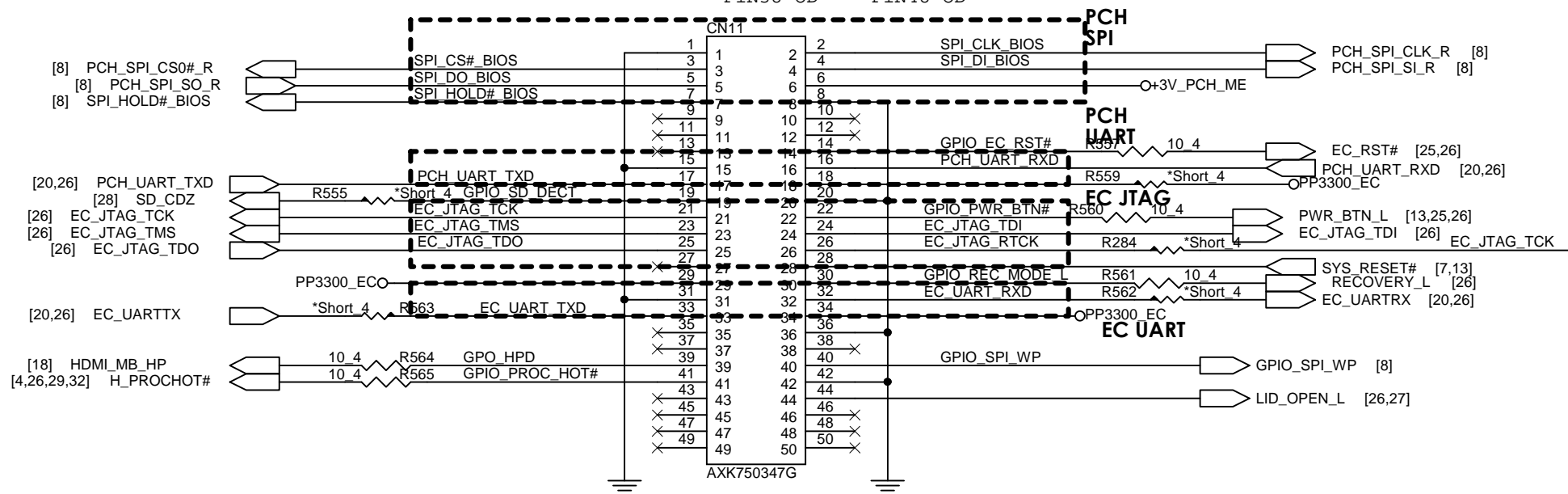
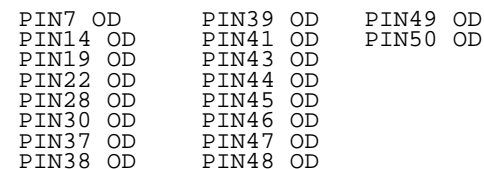
Touch Panel level shift(TPS)



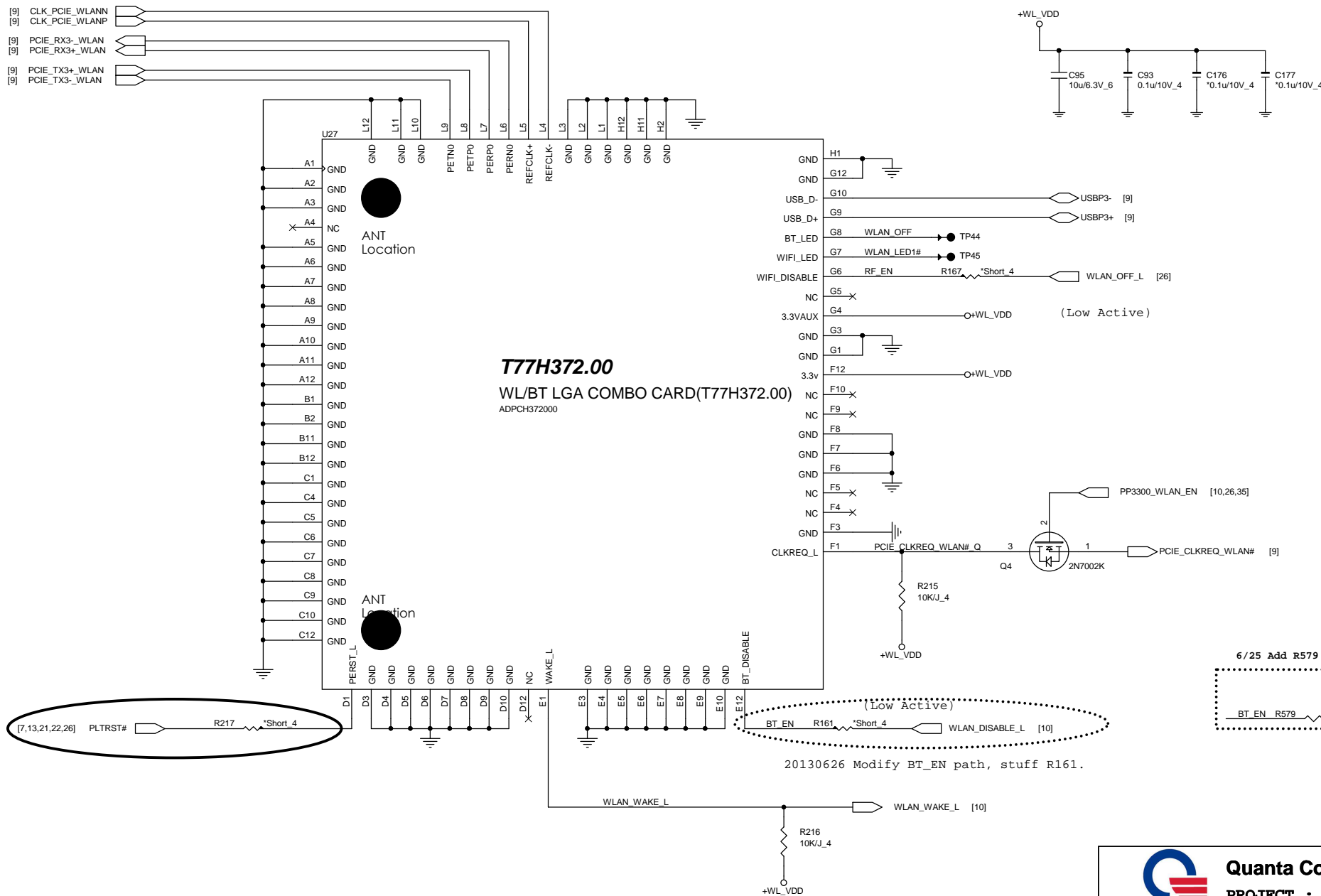
Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	LVDS/CCD/DMIC/TS	3B

Date: Monday, August 26, 2013 Sheet 16 of 39

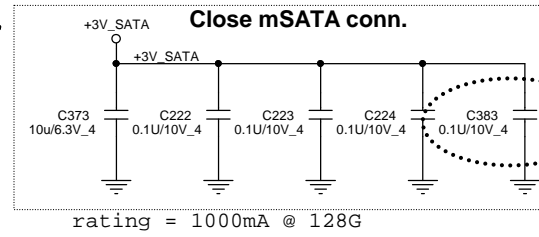
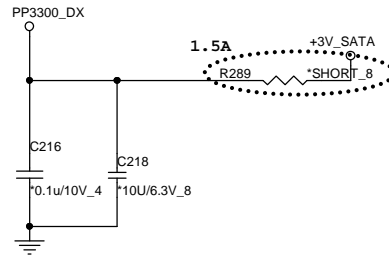


Size	Document Number	Rev
	Google Debug	3B
Date:	Monday, August 26, 2013	Sheet 17 of 39

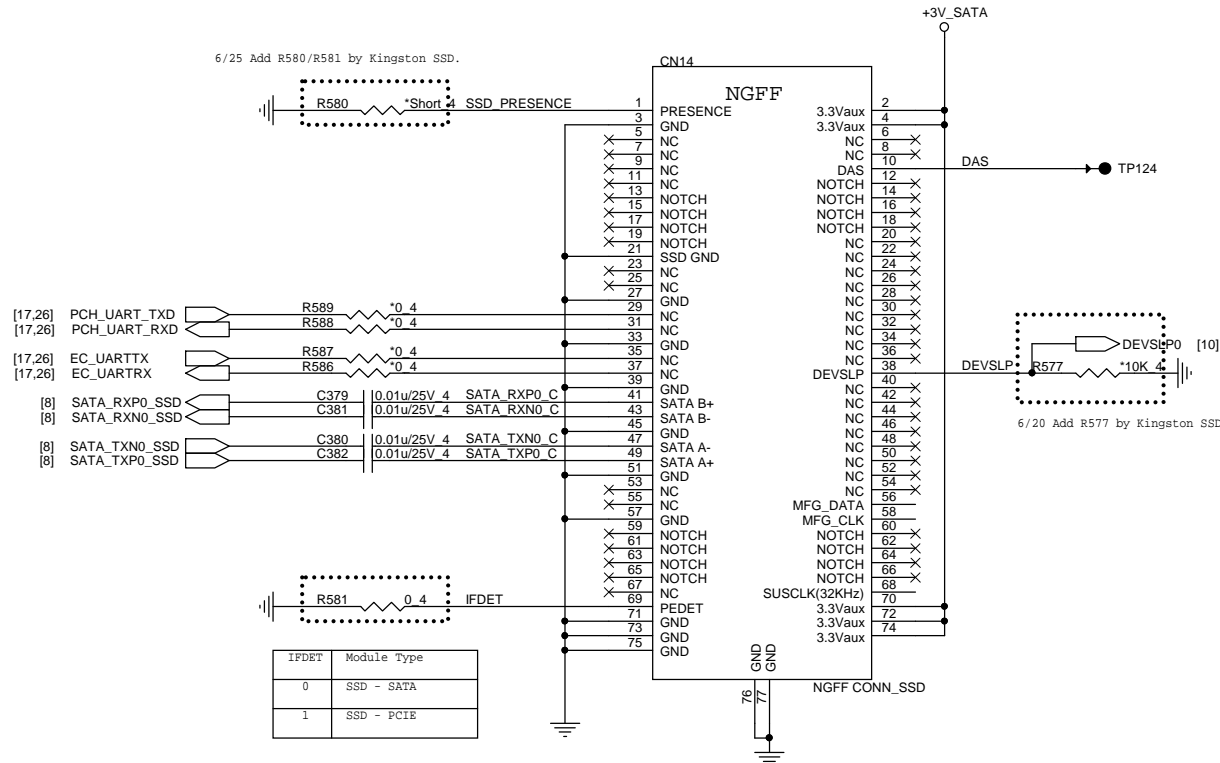


NGFF SSD connector. San Disk SSD Card.

20



20130521 Page20 Change CN14 to NGFF type.

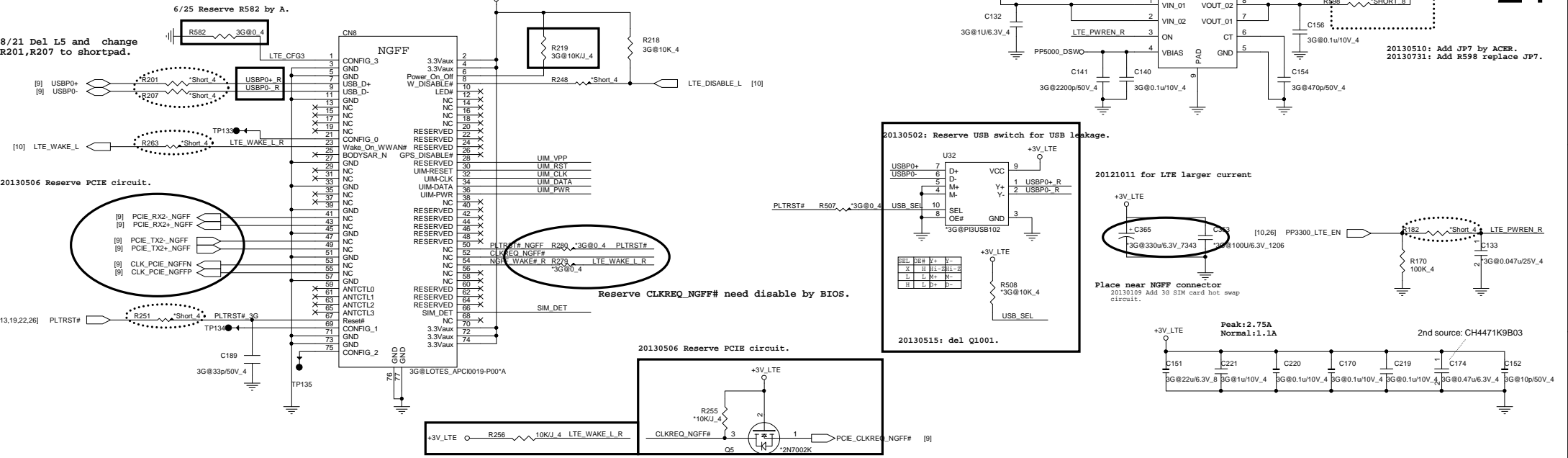


Quanta Computer Inc.

PROJECT : ZHN

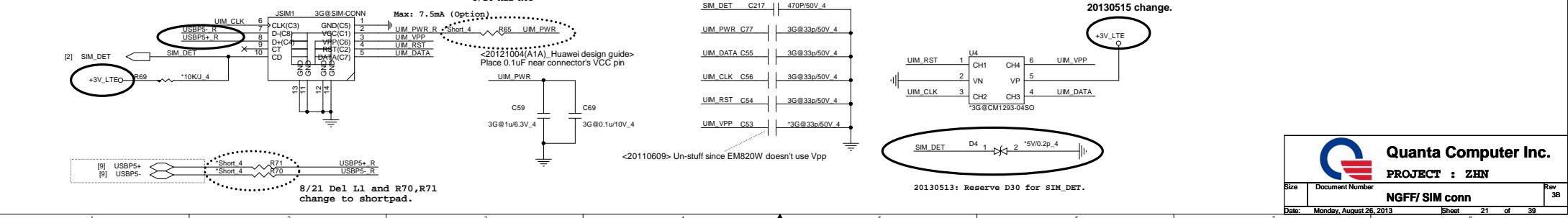
Size	Document Number	Rev
	NGFF SSD	3B
Date:	Monday, August 26, 2013	Sheet 20 of 39

NGFF 3G connector



MultiMedia SIM (MNC)

<Layout Notes> Keep USIM signals max length within 8000mils.



Quanta Computer Inc.

PROJECT : ZEN

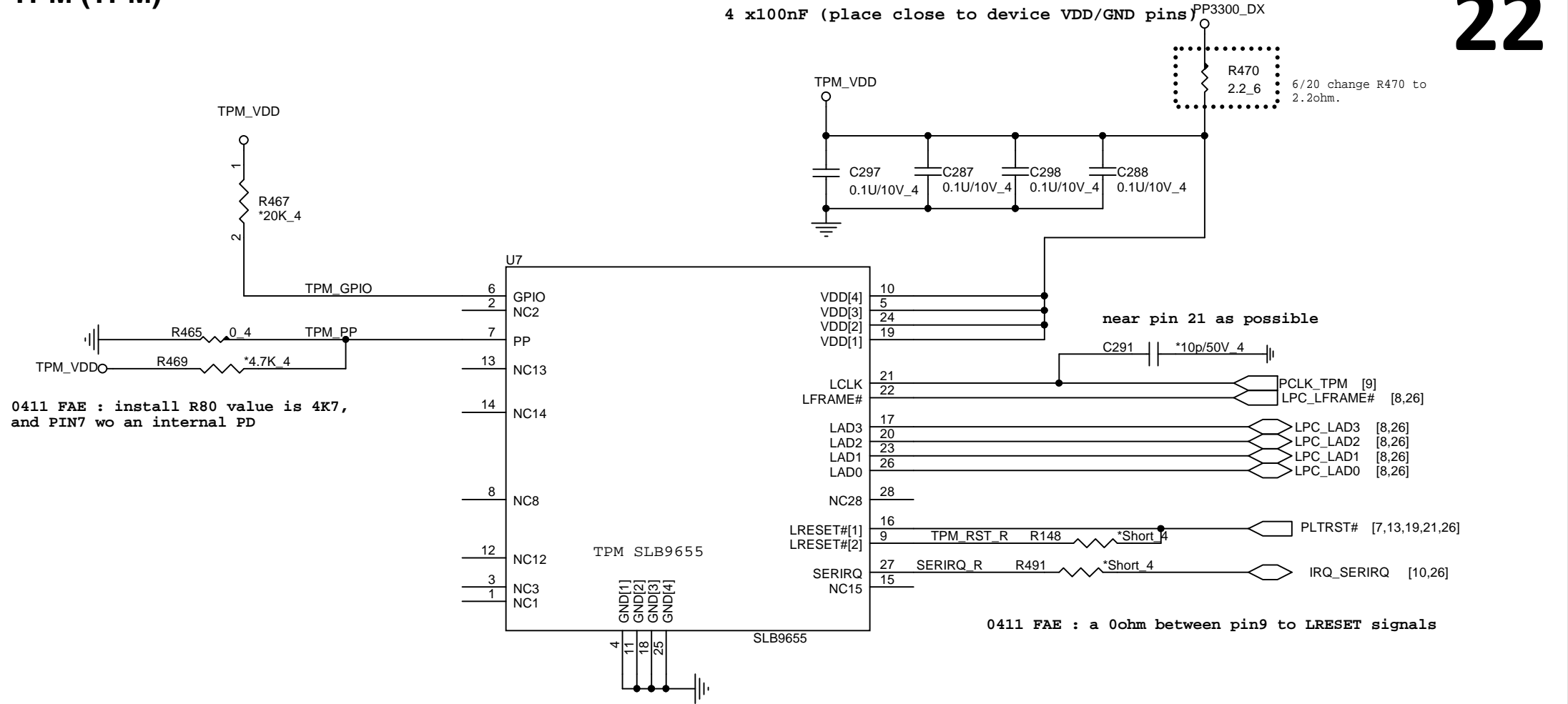
NGFF/SIM conn

Size Document Number Rev 3B

Date: Monday, August 26, 2013 Sheet 21 of 39

TPM (TPM)

22



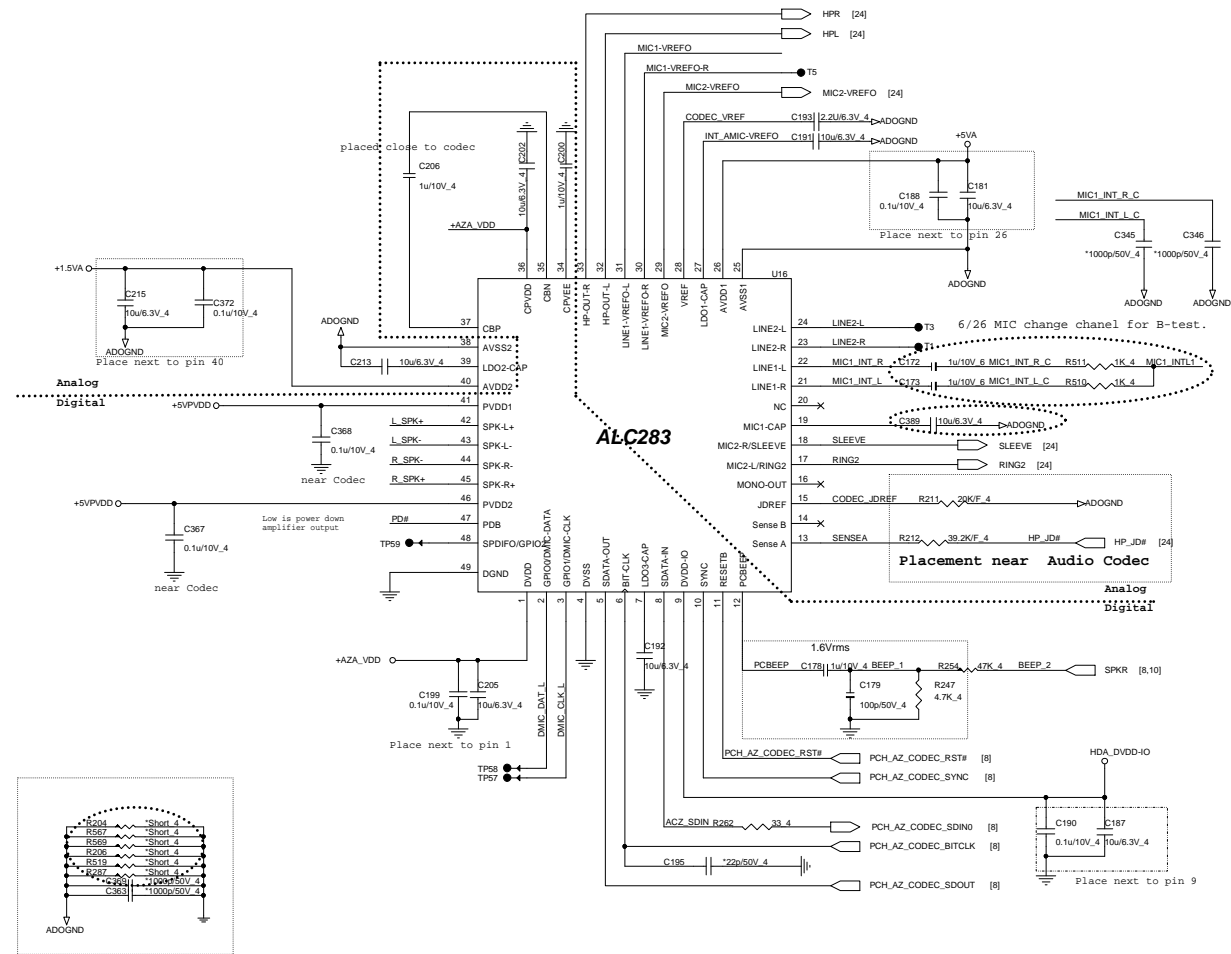
Quanta Computer Inc.

PROJECT : ZHN

Size	Document Number	Rev
	TPM SLB9655 / LED	3B

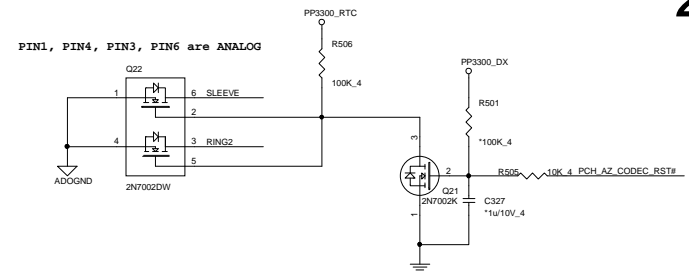
Date: Monday, August 26, 2013 Sheet 22 of 39

Codec(ADO)

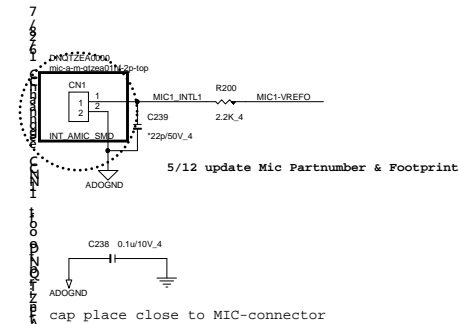


Grounding circuit(ADO)

23

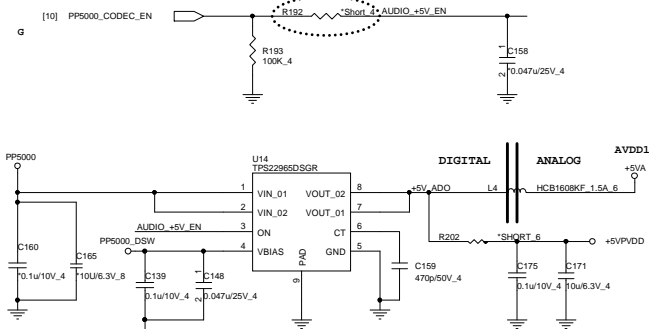


INT MIC array

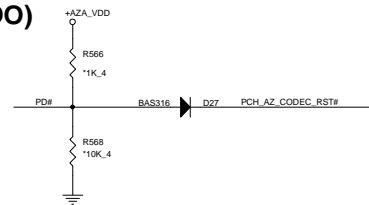


Codec PWR 5V(ADO)

5/31 RevB Del R195, C161.

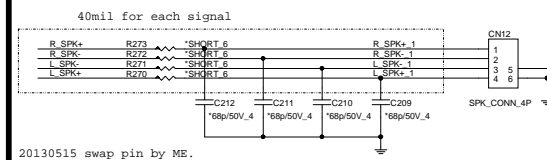


Mute(ADO)



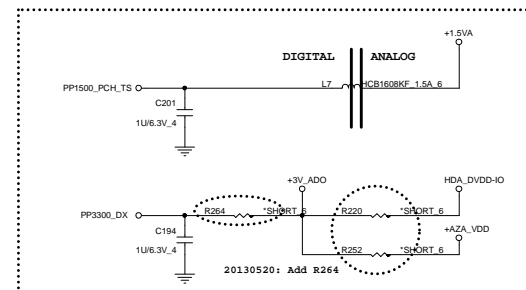
Internal Speaker

footprint 88266-040xx-xxx-4p-1



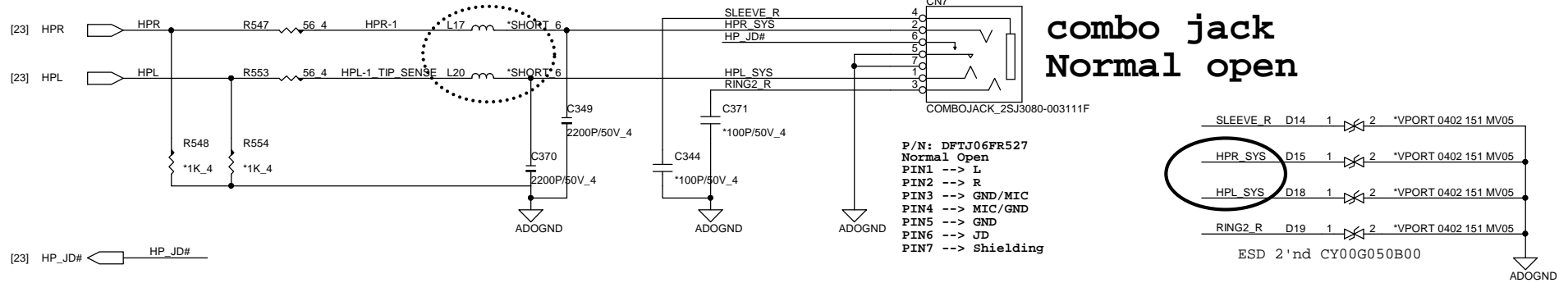
Codec PWR 3V/1.5V(ADO)

20130517 U13 remove, power source pass through to output.




HEADPHONE/Mic combo(ADO)

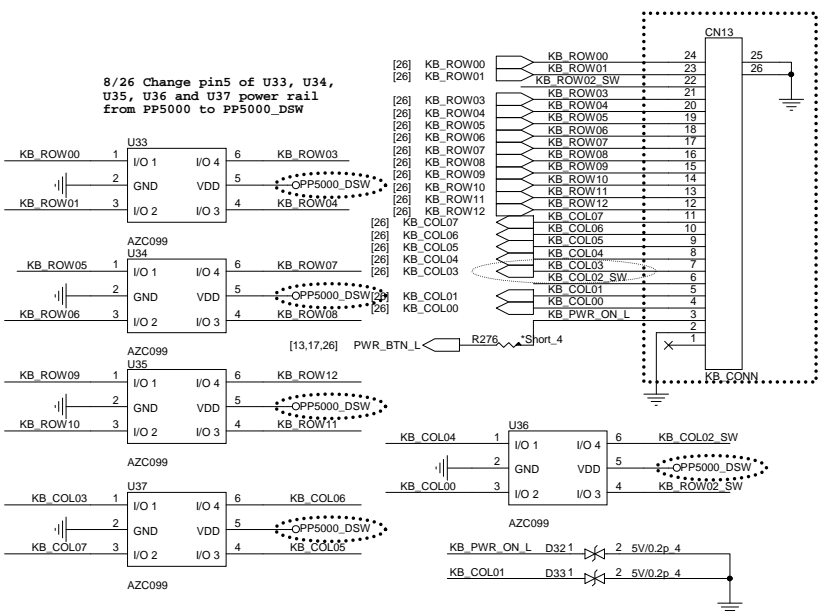
8/21 Change L16,L21 from
CX5PX800000 to 0ohm by SMT.



combo jack
Normal open

		Quanta Computer Inc.	
		PROJECT : ZHN	
Size	Document Number	Audio Headset SW	
Date: Monday, August 26, 2013	Sheet	24 of 39	Rev 3B

8/22 DFFC24FR098
footprint 88502-2401-24P-L-SMT

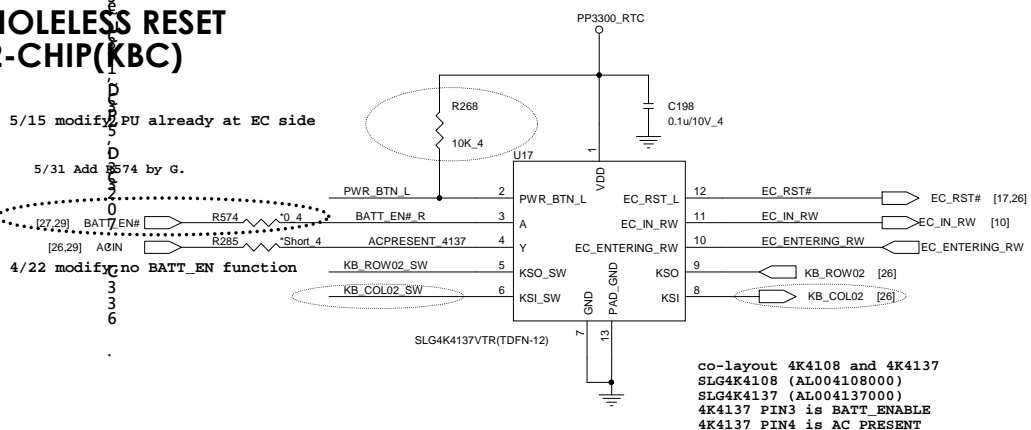


HOLELESS RESET 2-CHIP(KBC)

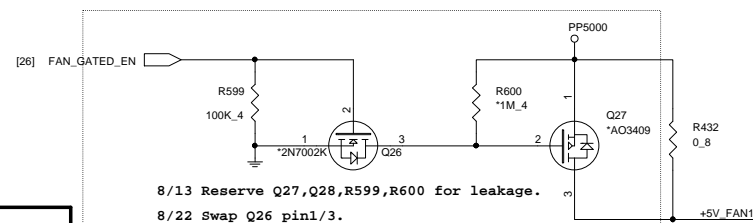
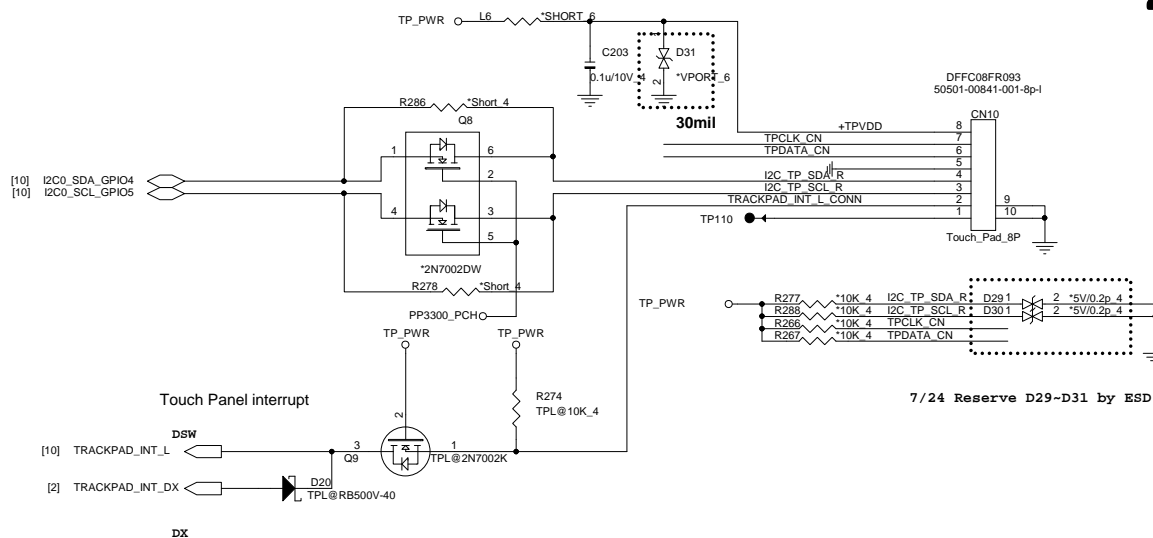
5/15 modify PU already at EC side

5/31 Add 3574 by G.

4/22 modify, no BATT_EN function

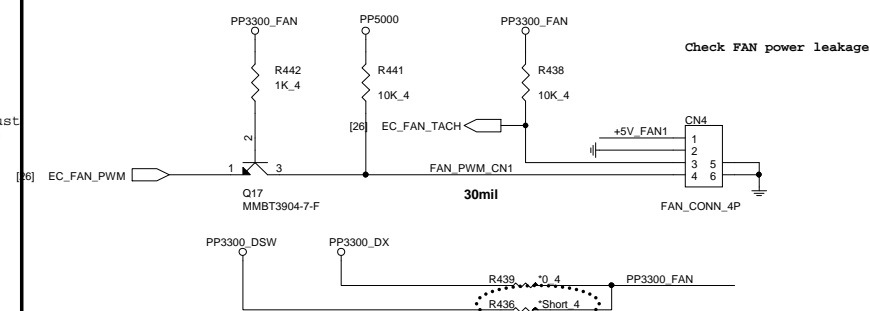


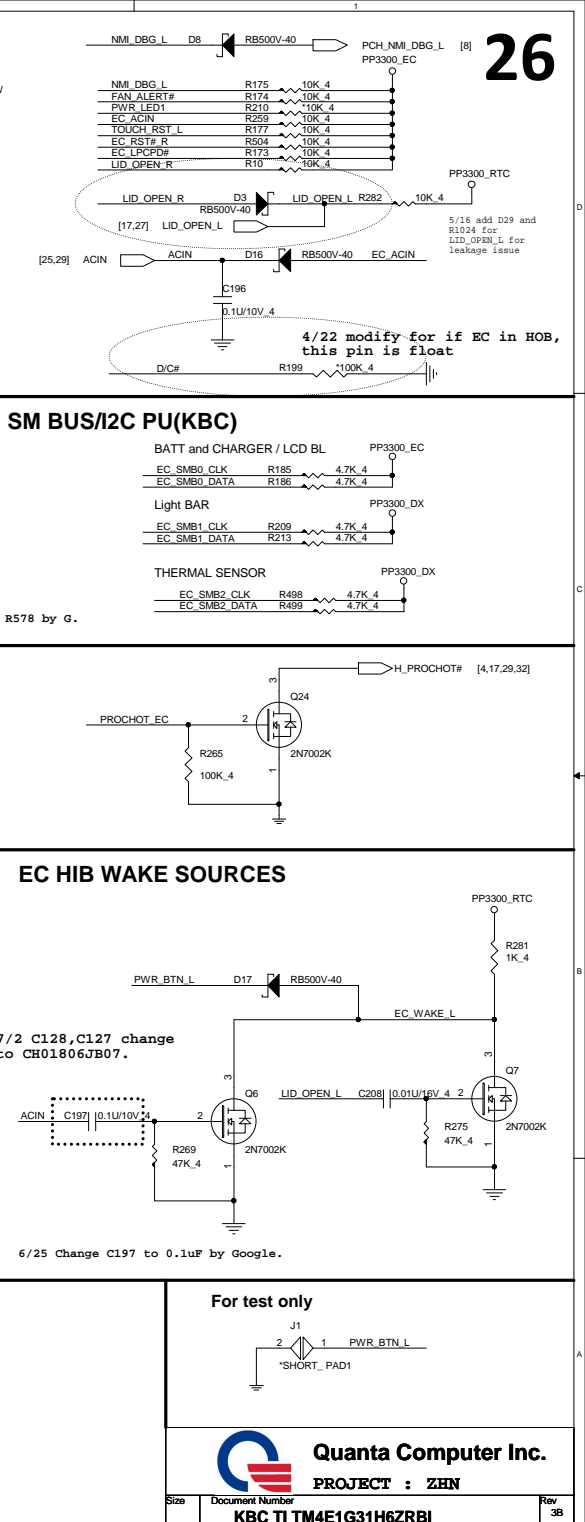
TOUCHPAD BOARD CONN (TPD)



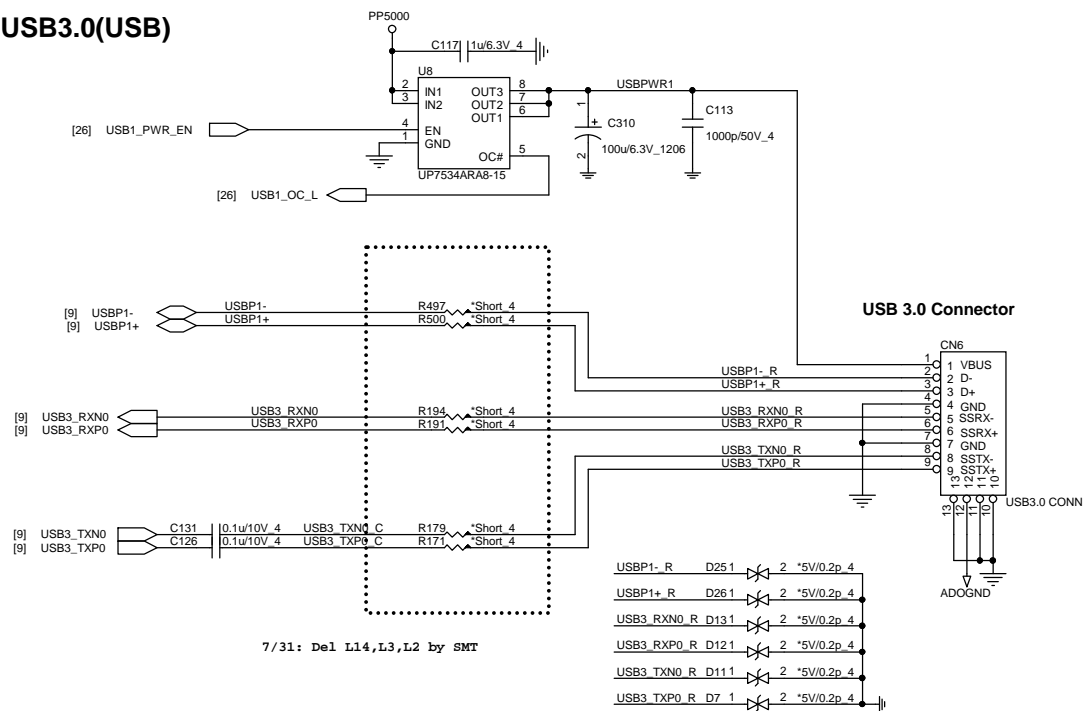
CPU FAN1 (THM)

```
Check pin define 0321
footprint 88266-040xx-xxx-4p-1
```

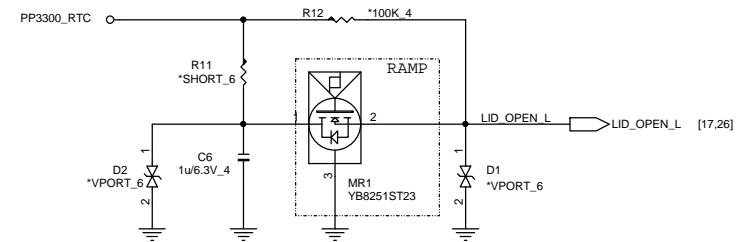




USB3.0(USB)



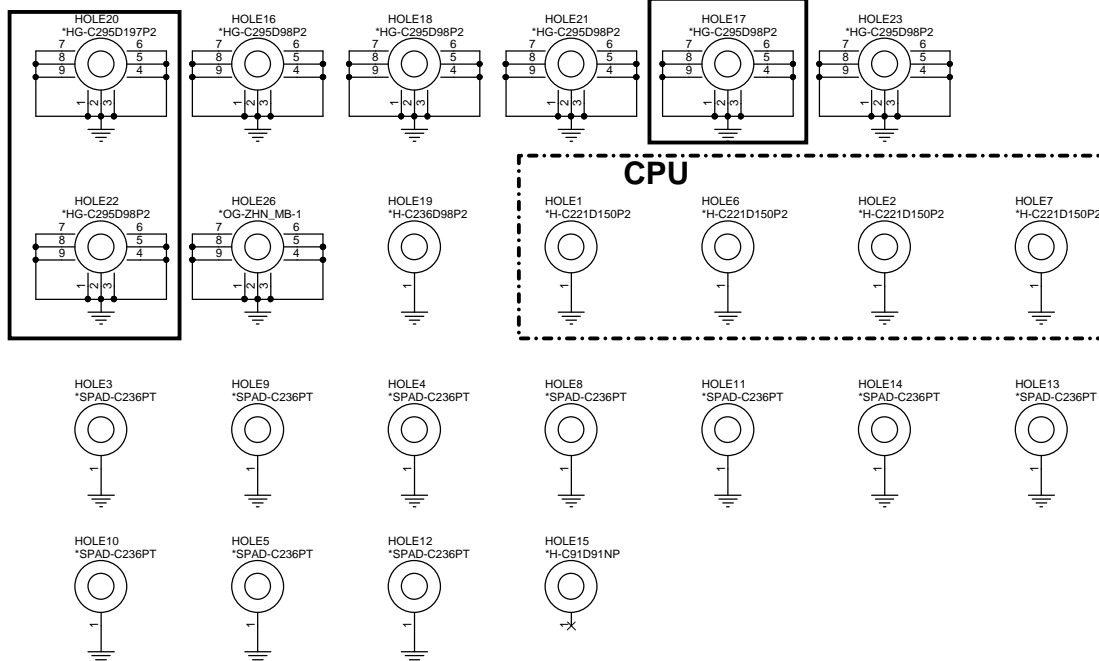
Lid Switch (HSR)



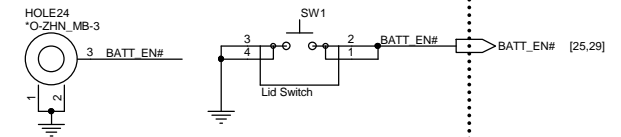
20130515 Add Hall IC by ME.

HOLE(OTH)

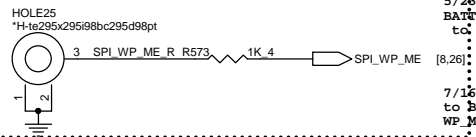
6/26 change footprint by ME.



BATT Enable short pad



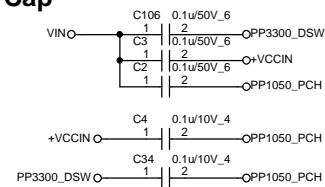
ROM WP#



5/28: Change hole24 from BATT_EN# to SPI_WP_ME; Add R573

7/16: modify Hole17; Hole24 to BATT_EN#; Hole25 to SPI_WP_ME

EMI Cap



20130520: Add C6417, C6418, C6419, C6420, C6421

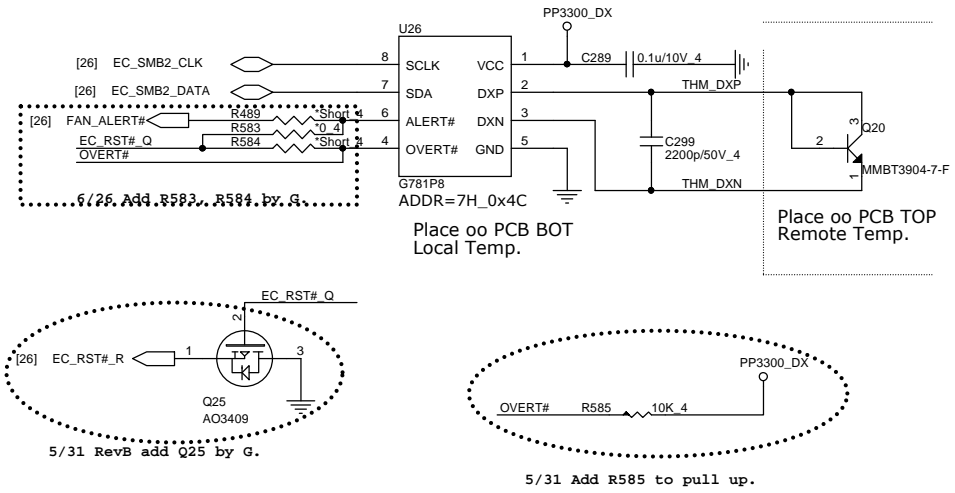


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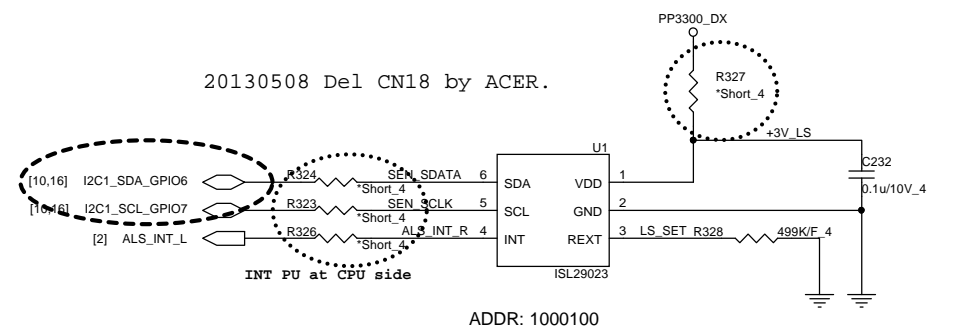
PROJECT : ZHN

Size	Document Number	Rev
	USB3/Hole	3B
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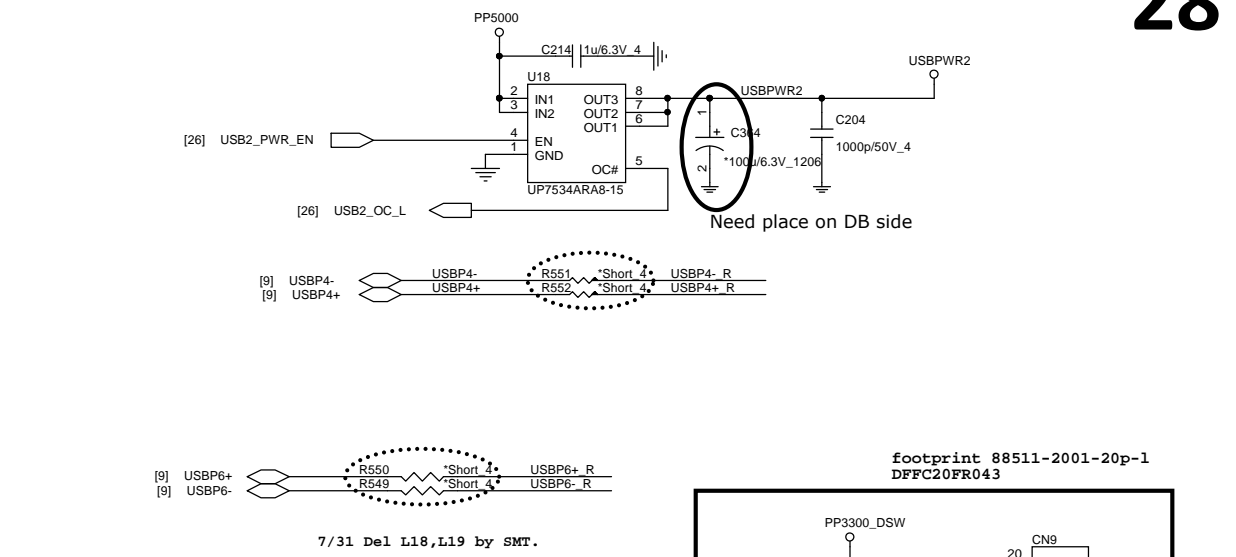
Thermal Sensor(THM)



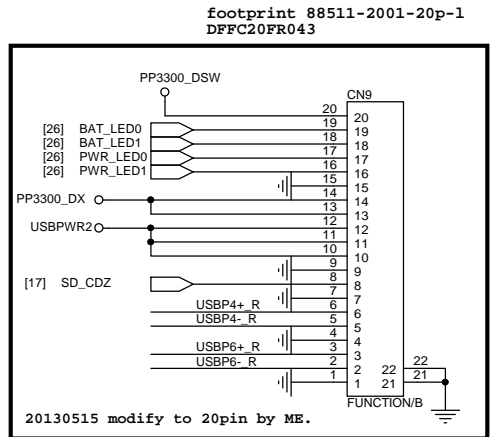
Light sensor & TP (SER)



FUNCTION DB



HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2

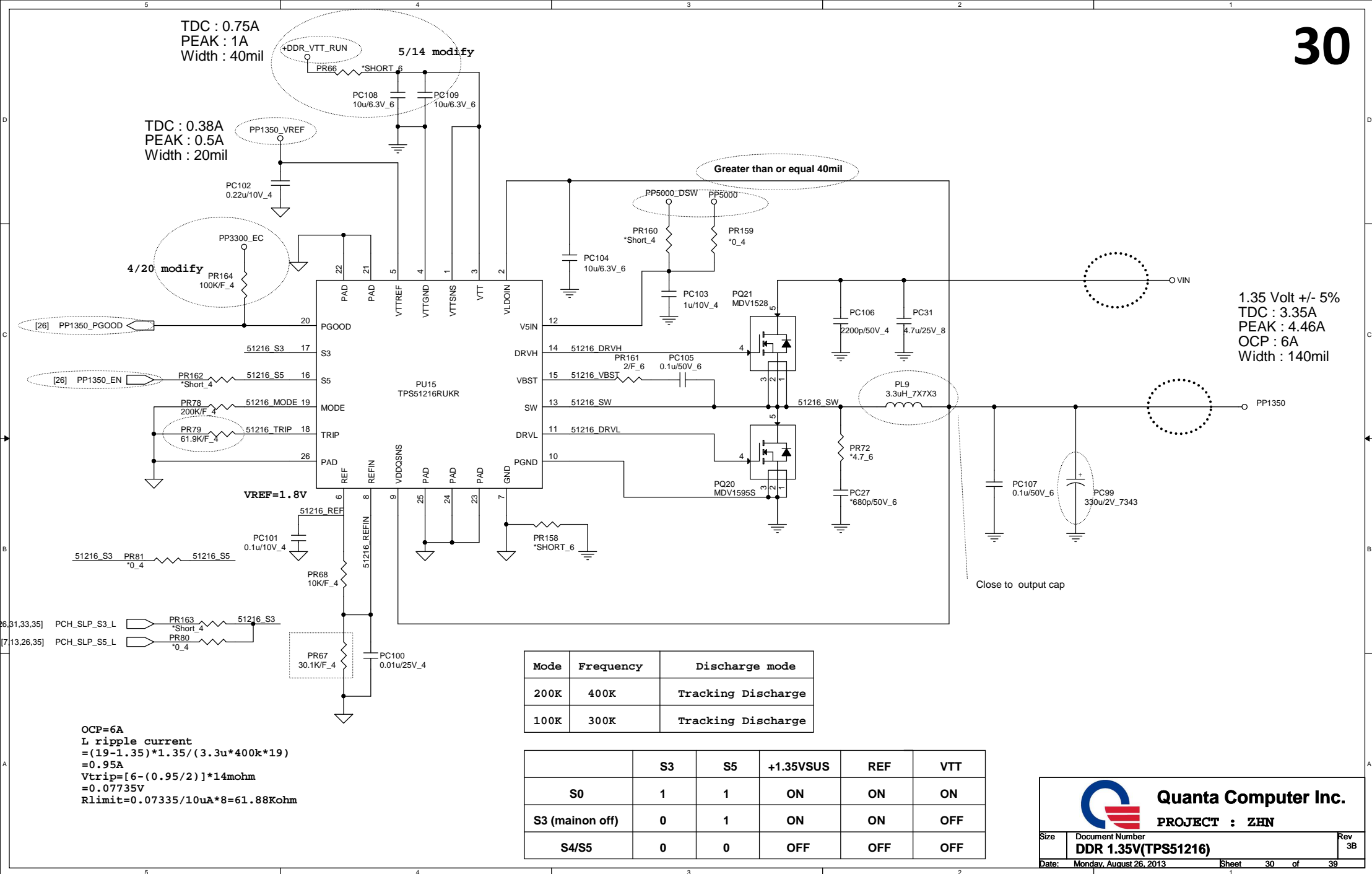


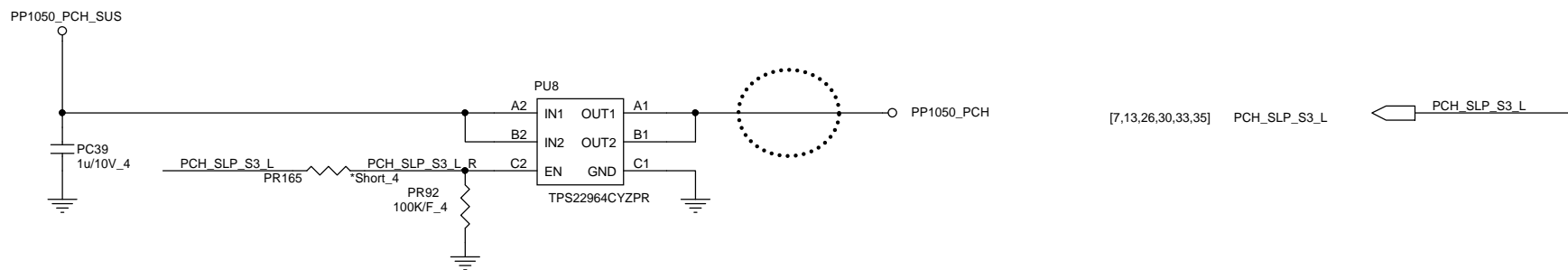
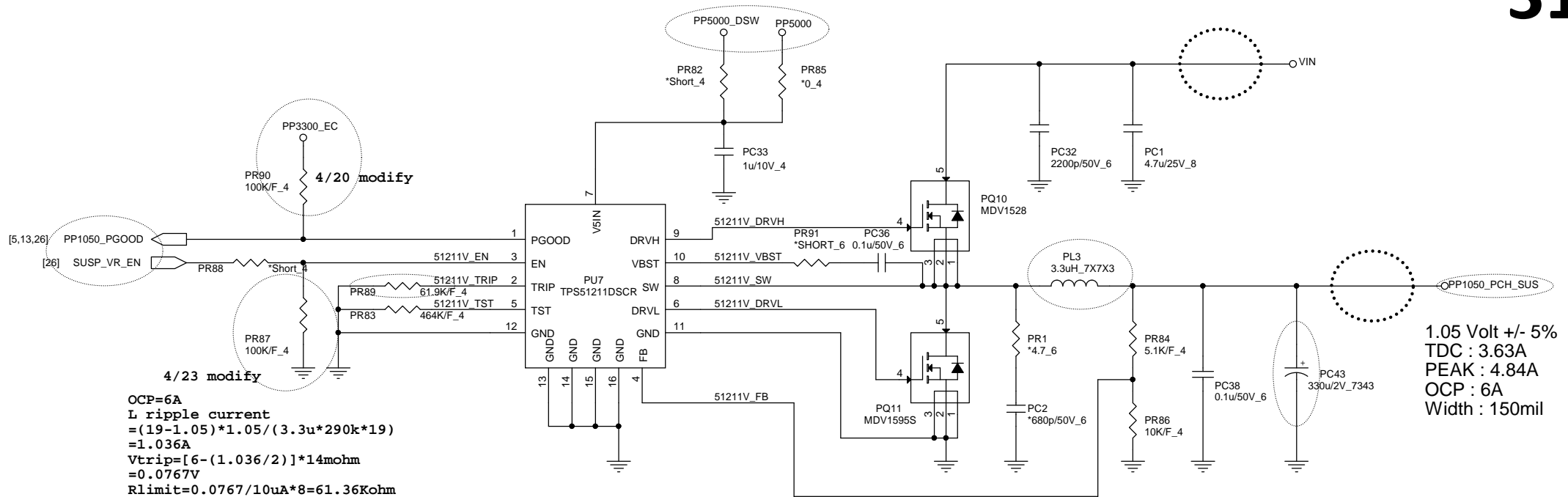
Quanta Computer Inc.

PROJECT : ZHN

Size	Document Number	Rev
	DB/ALS/Thermal sensor	3B

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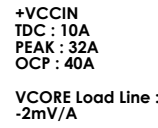


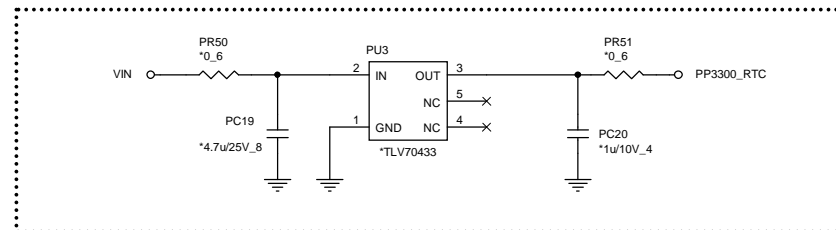
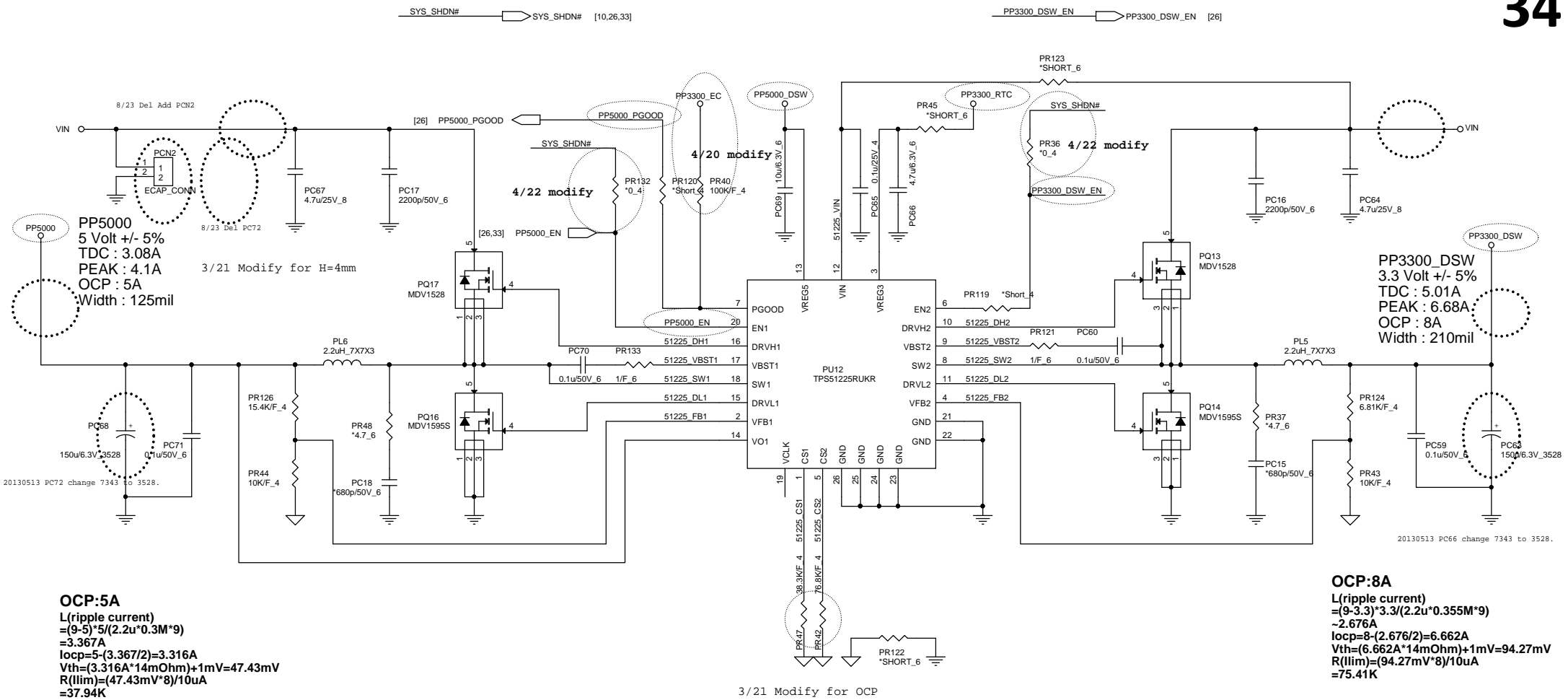


Quanta Computer Inc.
PROJECT : ZHN

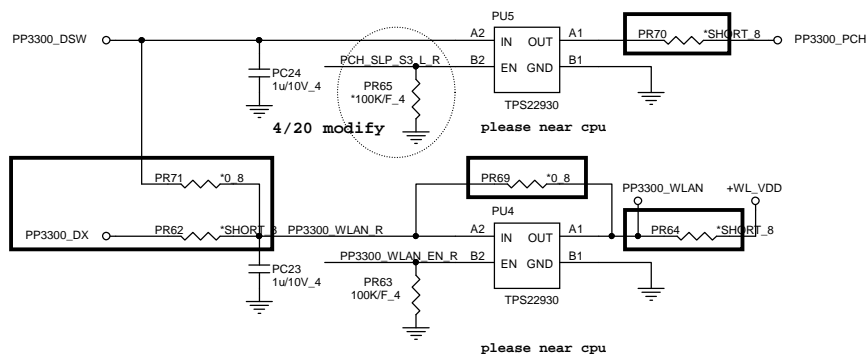
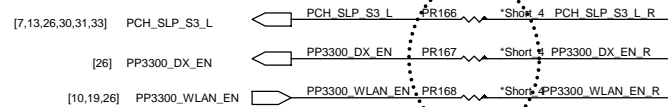
Size	Document Number	Rev
	+1.05V(TPS51211)	3B

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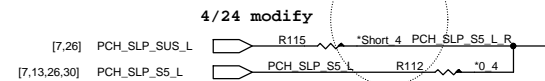
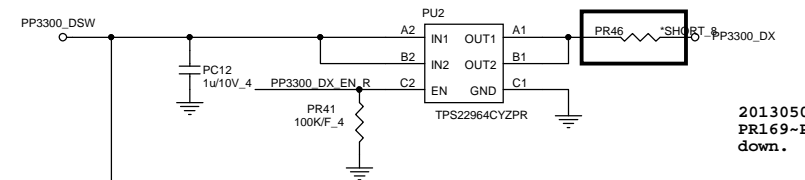


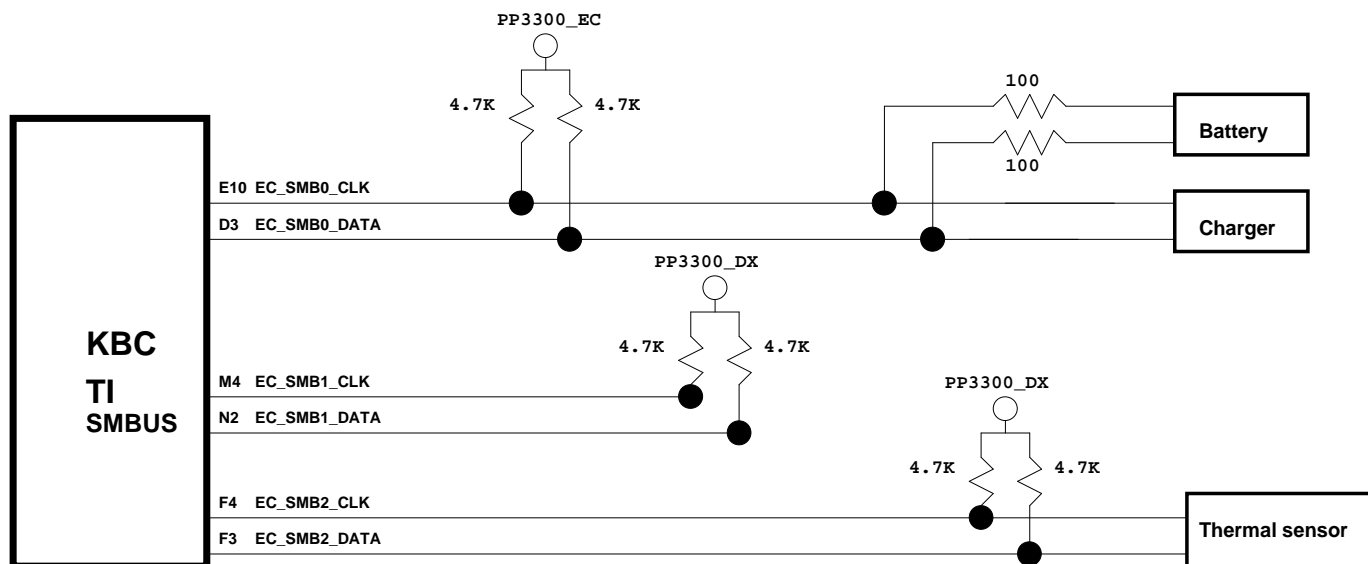
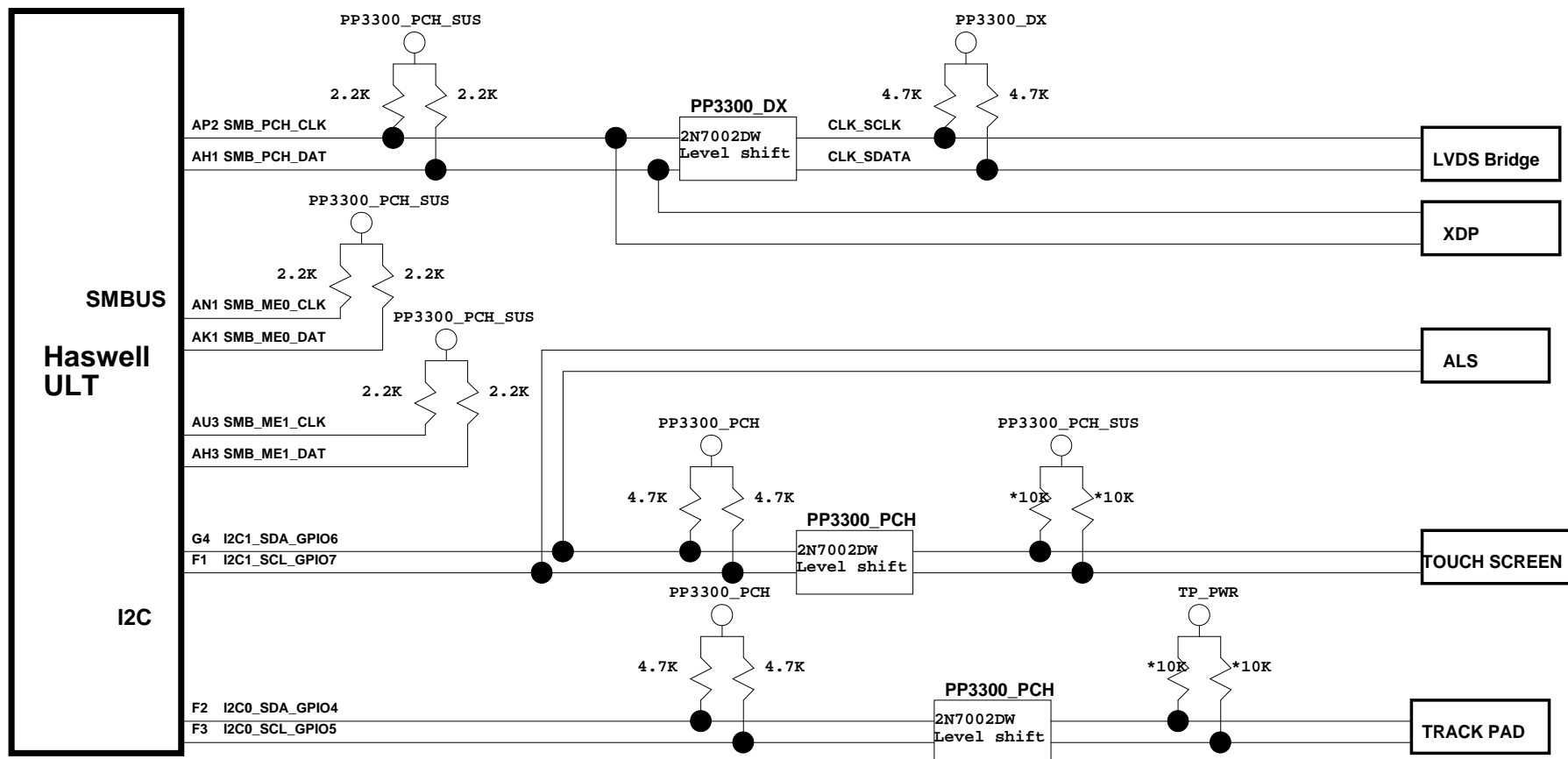


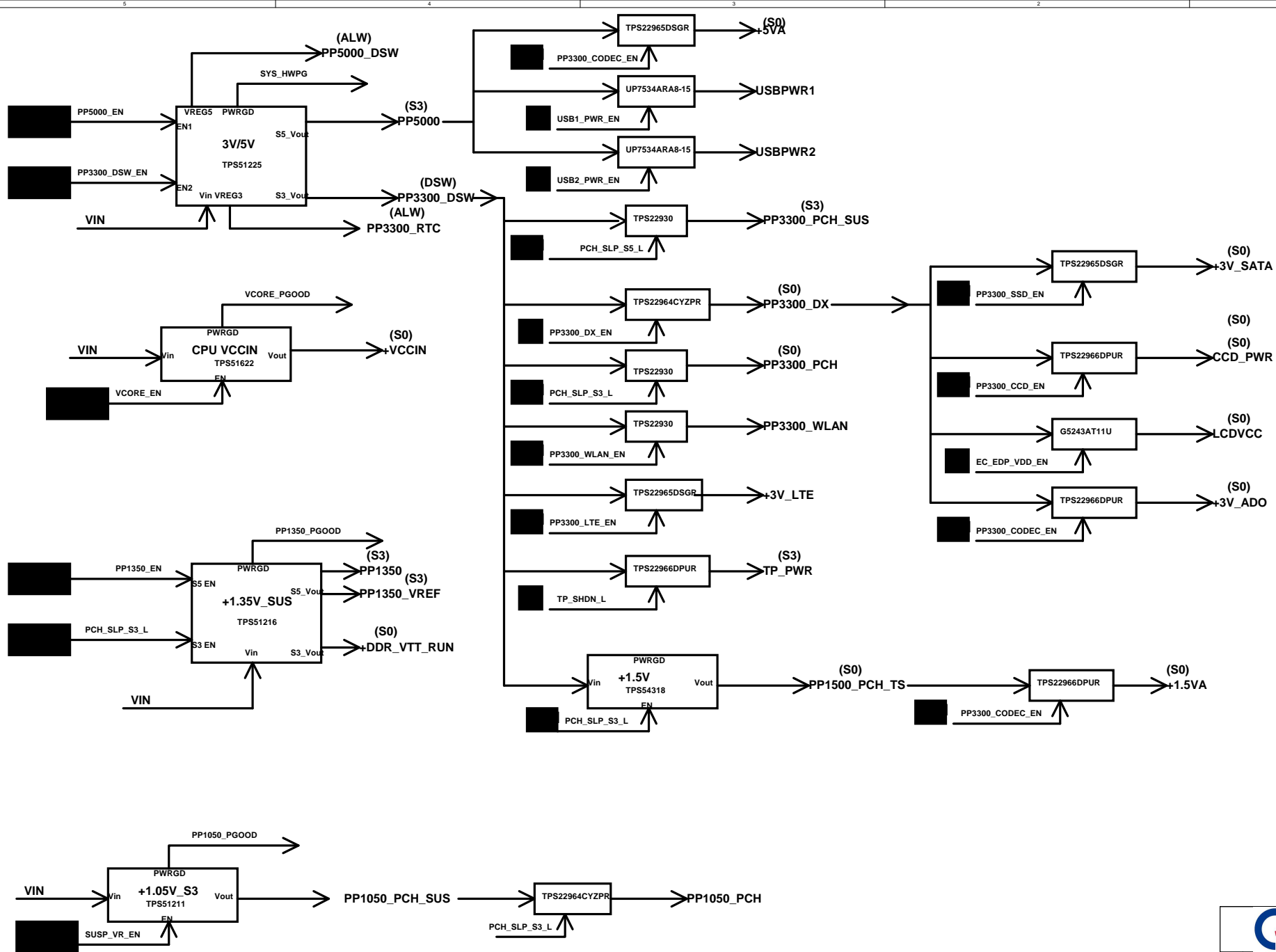
6/23 Add PR166~168 for debug.



20130517 Page35 Add PR174 & reserve PR175,PR176 to input pwr PU4 by ACER.







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